Pioneer-Central

FREQUENCY TEMPERATURE COMPENSATION TECHNIQUES FOR QUARTZ CRYSTAL OSCILLATORS

SECOND QUARTERLY REPORT

PIONEER-CENTRAL DIVISION
DAVENPORT, IOWA

THE Bendix CORPORATION

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RESEARCH WORK FOR FREQUENCY TEMPERATURE COMPENSATION TECHNIQUES FOR QUARTZ CRYSTAL OSCILLATORS

in conjunction with Signal Corps

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CONTRACT NO. DA36-039 SC-90782

REPORT NO.2

Object of Research: The design and development of circuit techniques for oven-less crystal oscillators having frequency temperature stabilities previously achieved in temperature stabilized oscillators consuming several watts of power

Prepared for
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and
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1.1 Purpose

The purpose of this project is to evolve a practical analytical and empirical approach to the temperature compensation of a quartz crystal oscillator. The study will encompass numerous methods of compensation, of which the most promising will be investigated fully and complete design procedure obtained. The study will be concentrated on a nominal frequency of three megacycle, but will be generally applicable to AT cut quartz crystal of from 1 to 20 megacycles.

2.1(a) Abstract

The different methods of frequency-temperature compensation (varicap, transistor and isolation stage, binistor, and capacitor-diode) are discussed. New techniques and approaches to compensation of crystal oscillators are presented, and mathematical analyses are developed for each. Empirical data is presented indicating the characteristics of each compensation method. A method of obtaining negligible effect of B+ voltage changes is presented.

Several new approaches to voltage control networks are discussed, including a bridge voltage and current control network that is applicable to both the varicap and capacitor-diode method.

Aging data on four oscillators is presented which is a continuation of the aging tests started during the first quarter of this contract. The aging oscillators were temperature cycled and the original frequency-temperature characteristics were compared to the characteristics obtained.

2.1(b) Conferences

Mr. Owen P. Layden of the Signal Corps visited Pioneer-Central Division of The Bendix Corporation on 12 December 1962. During this conference progress on Contract No. DA36-039 SC-90782 was reviewed.

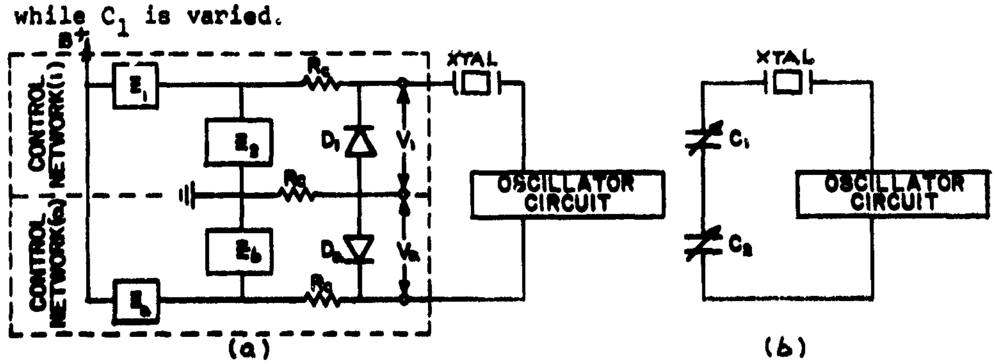
After reviewing the progress, Mr. Layden suggested several circuit modifications be investigated with the results shown in subsequent reports.

The conference also included the proposed investigation efforts for the third quarter.

3.1 Varicap Method

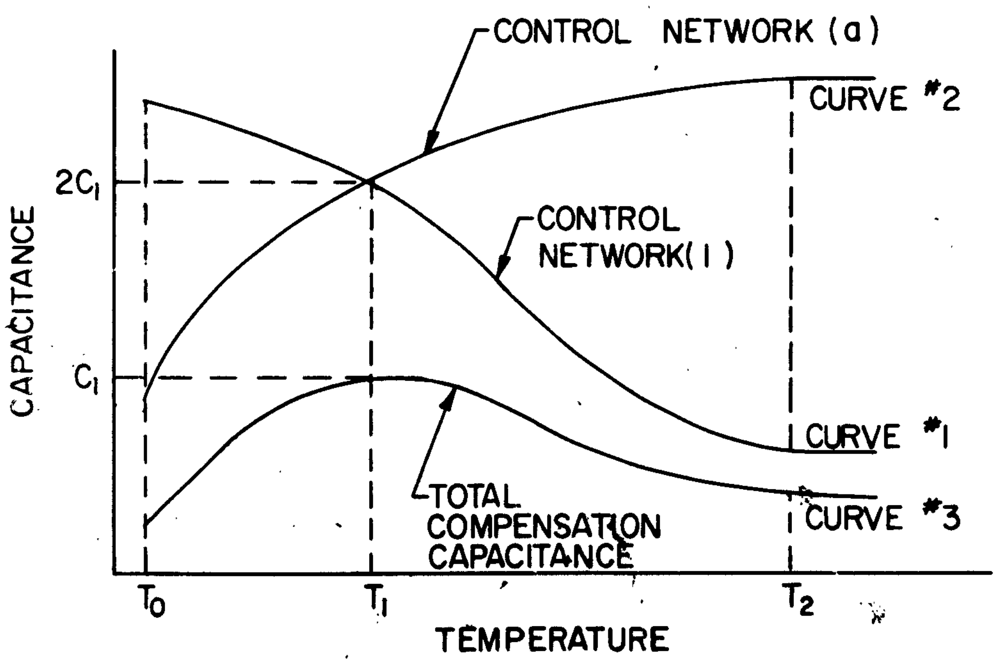
The First Quarterly Report contained the basic theory of the varicap method. During the second quarter, emphasis has been placed on investigation of the characteristics of compensation techniques and circuit designs. Investigation was conducted on the use of two varicaps and compensation networks, a bridge compensation circuit with a varicap, and zener diode control of voltages generated by thermistor-resistor networks. Effort was also conducted on optimizing the oscillator circuit parameters and on investigating the required compensation networks using different cuts of crystals and different values of varicaps.

The idea of utilizing two varicaps and two compensation networks has been investigated. The following circuit, Figure 3.1.1(a) illustrates an oscillator using this method. D_1 and D_a are voltage variable capacitors. Z_1 and Z_2 are the voltage control elements for D_1, and Z_a and Z_b are the voltage control elements for D_a, Figure 3.1.1(b) is the equivalent electrical diagram for Figure 3.1.1(a). The variable capacitance, C_1, is the capacitance of diode D_1 controlled by Z_1 and Z_2 and the variable capacitance, C_2, is the capacitance of diode D_a controlled by Z_a and Z_b. C_1 and C_2 are independent of each other. C_1 can be made constant while C_2 is varied or C_2 can be made constant while C_1 is varied.



TWO VARICAP COMPENSATION CIRCUIT
Figure 3.1.1

Figure 3.1.2, Curve #3, is a typical plot of C versus temperature that is required to compensate an AT cut crystal. The difficulty encountered when using only one varicap and thermistor network, Z_1 and Z_2, is that to generate the slope from temperature T_o to T_1 requires the thermistor-resistor network resistance of Z_2 to decrease very rapidly with temperature. The change in slope at temperature T_1 and from T_1 to T_2 requires that Z_1 decrease very rapidly with temperature. The decrease in Z_1 must also offset the decrease in Z_2 past T_1, just as the increase in Z_2 must offset the increase in Z_1 below T_1. This interaction of Z_1 and Z_2 around the temperature T_1 makes the matching of the curve around the T_1 temperature difficult in many cases. By using two independent control elements, this problem can be reduced or even eliminated.



COMPENSATION CAPACITANCE VS TEMPERATURE
FOR TWO VARICAP COMPENSATION METHOD
Figure 3.1.2

The equivalent capacitance of the two diodes shown in Figure 3.1.1(a) can be expressed as follows. K_1 and K_2 are constants determined by the type of diode used.

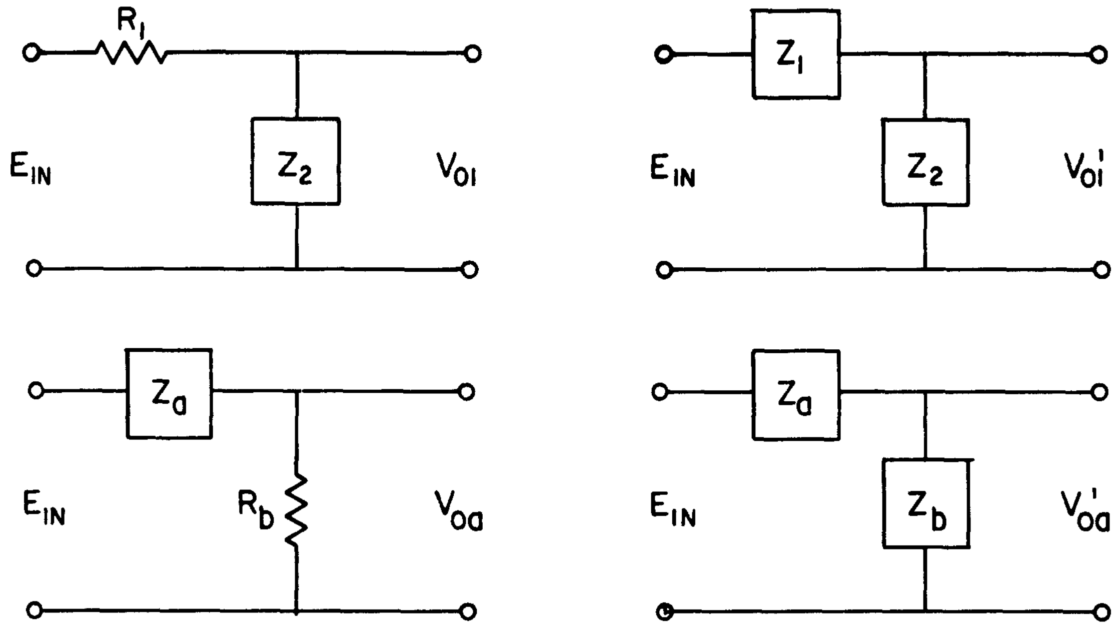
$$1)\quad C_x = \frac{C_1 \; C_a}{C_1 + C_a}$$

$$2)\quad C_1 = \frac{K_1}{\sqrt{V_1}}$$

$$3)\quad C_a = \frac{K_a}{\sqrt{V_a}}$$

$$4)\quad C_x = \frac{1}{\dfrac{\sqrt{V_a}}{K_a} + \dfrac{\sqrt{V_1}}{K_1}}$$

Assume that D_1 has control from T_o to T_1 and D_a has control from T_1 to T_2. Then the curve of capacitance versus temperature for each one must be as shown in Figure 3.1.2, Curves #1 and #2. As can be seen, the slope of C versus temperature must change magnitude rather abruptly, but the slope does not have to change sign as in the one varicap compensation circuit. As indicated in Figure 3.1.3(a), only one thermistor network in each compensation circuit is required to generate C_1 and C_2 versus temperature curves similar to the ones shown in Curves #1 and #2 of Figure 3.1.2. Although only one thermistor network may be required, the change in capacitance may be difficult to generate at T_o. Therefore, thermistor networks, Z_1 and Z_b, are included for R_1 and R_b as shown in Figure 3.1.3(b). Z_1 does not have any effect below T_1, and Z_b does not have any effect above T_1. The only function performed by Z_1 and Z_b is to maintain V_o constant or nearly constant when either compensating capacitor goes beyond its specified temperature range.

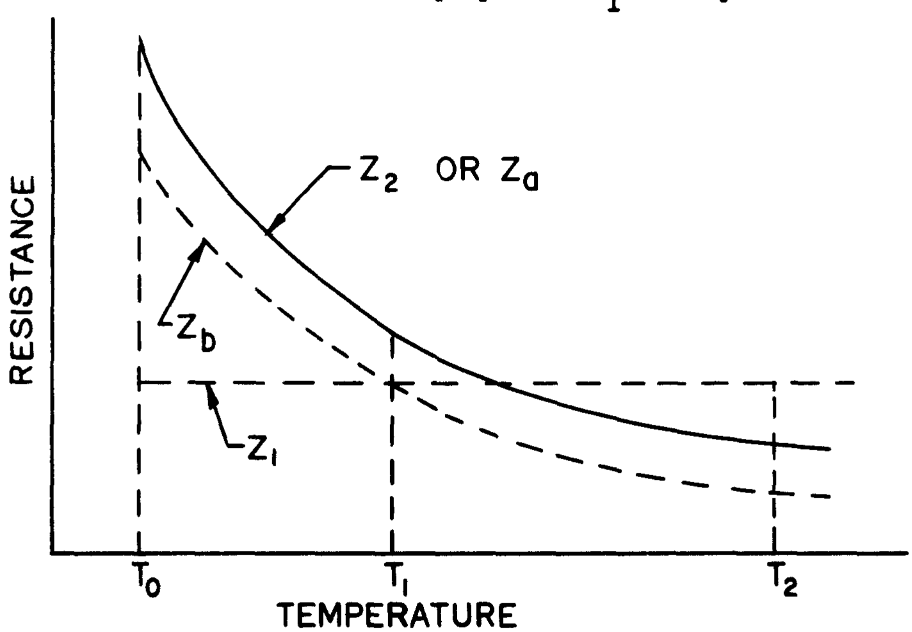


(a)
COMPENSATION NETWORKS FOR
TWO VARICAP METHOD

(b)
MODIFIED COMPENSATION NETWORKS
FOR TWO VARICAP METHOD

Figure 3.1.3

Figure 3.1.4 illustrates the purpose of Z_1 at temperature above T_1.



CORRECTION CURVES TO ELIMINATE
INTERACTION OF TWO COMPENSATION NETWORKS
Figure 3.1.4

At T_1 and above, where C_1 is required to be constant, Z_1 changes in such a manner that the change in Z_2 is cancelled. The following equations show the relationship that must exist between Z_1 and Z_2 from T_1 and T_2.

$$5)\quad V_o = \frac{Z_2}{Z_1 + Z_2}(E)$$

$$6)\quad \frac{dV_o}{dZ_1} = \frac{Z_1}{(Z_1 + Z_2)^2}(E)$$

$$7)\quad \frac{dV_o}{dZ_1} = \frac{Z_2}{(Z_1 + Z_2)^2}(E)$$

To maintain V_o constant from T_1 and T_2,

$$8)\quad \frac{Z_1(dZ_2)}{(Z_1+Z_2)^2}(E) = \frac{Z_2(dZ_1)}{(Z_1 + Z_2)^2}(E)$$

$$9)\quad \frac{dZ_1}{dZ_2} = -\frac{Z_1}{Z_2}$$

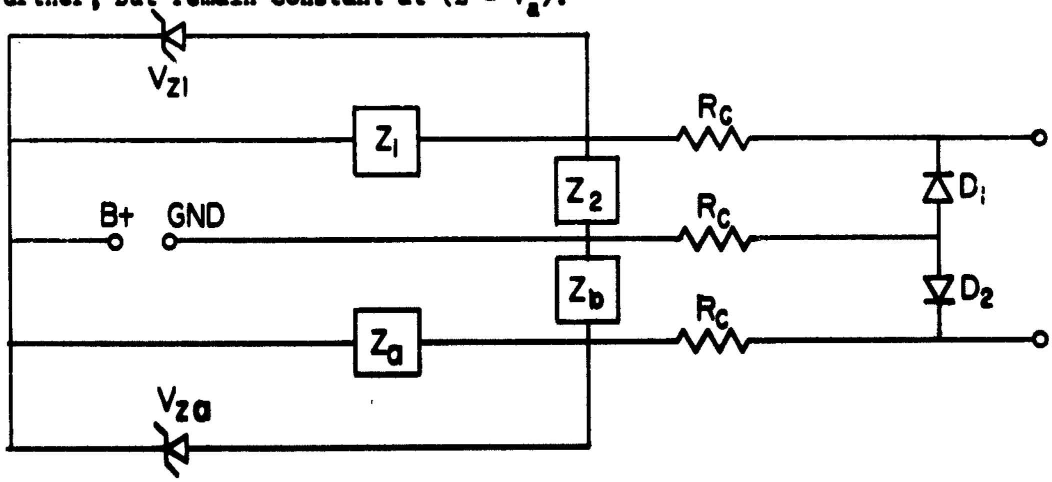
Therefore, the rate of change of Z_1 with respect to Z_2 must be $(-Z_1/Z_2)$ to maintain a constant voltage, V_o is shown by Equation 10.

$$10)\quad dZ_1 = -\frac{Z_1}{Z_2}(dZ_2)$$

The problem now reduces to providing a thermistor-resistor network that does not vary from T_o to T_1 and changes at the rate of $-Z_1/Z_2(dZ_2)$ from T_1 to T_2.

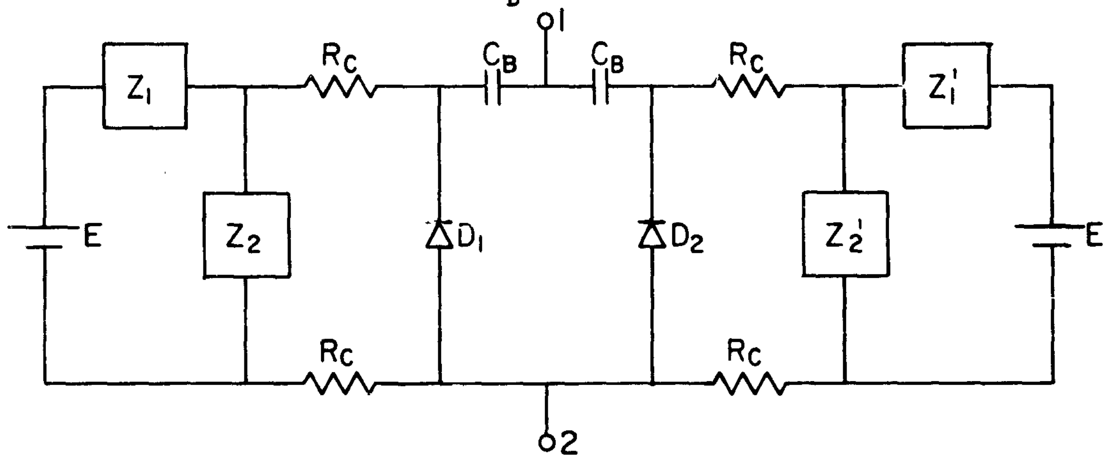
Equation 10 can be rather complicated if Z_1 is different in magnitude by a larger factor than Z_2 at T_o, but if, as is usually the case, Z_1 is approximately of the same magnitude as Z_2, then the ratio of $-Z_1/Z_2$ at T_1 can be used for $(-Z_1/Z_2)$ from T_1 to T_2 with little effect. The analysis presented above can be used to determine the requirements for Z_1 and Z_b.

A possible method of generating the required capacitance versus temperature curves shown in Figure 3.1.2 is to use zener diodes in the compensating networks. Figure 3.1.5 is an example of how zener diodes can be used to generate the required voltage versus temperature curves. The operation of a single compensating circuit using zener-diode control was explained in the First Quarterly Report. As Z_2 decreases in resistance with temperature, the voltage across Z_1 increases to some value V_1. If the zener diodes has its knee at V_1, then the voltage cannot increase beyond V_1 and V_o remains constant at temperatures above T_1. As Z_a increases as temperature decreases, the voltage V_{o2} decreases and the voltage across Z_a increases to some maximum voltage, V_a. At the temperature T_1, V_{o2} has decreased to its minimum value. If the zener diode across Z_a is at V_a, then the output V_{o2} cannot decrease further, but remain constant at $(E - V_a)$.



ZENER CONTROL OF TWO VARICAP COMPENSATION NETWORK
Figure 3.1.5

Another two varicap method that can be used for compensation is to parallel the varicaps as shown in Figure 3.1.6. D_1 and D_2 are varicaps, the Rc's are decoupling resistors; the C_B's are d-c blocking capacitors and



TWO DIODE PARALLEL COMPENSATION NETWORK
Figure 3.1.6

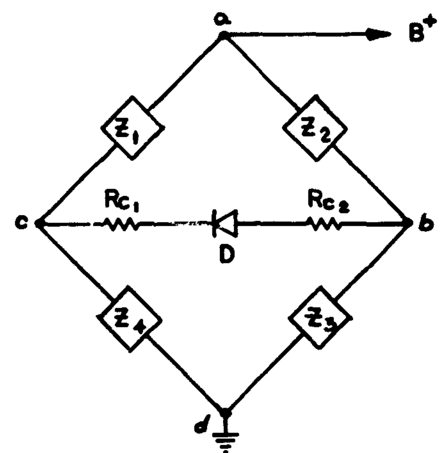
Z_1, Z_2, Z_1' and Z_2' are the temperature sensitive control networks. The equation for the capacitance at the terminals 1-2 is simply:

$$11)\quad C_x = C_1 + C_2$$

Assuming that the capacitance to be simulated by this network is as shown in Figure 3.1.2, Curve #3, the individual capacitance could vary with temperature in a similar manner as shown in Figure 3.1.2, Curves #1 and #2, but the magnitude of each individual network will be about one fourth as much as shown for the series network. The same reasoning as used for the series varicap method can be used to show that zener diode control will be advantageous around the temperature T_1.

Due to the fact that only voltage divider circuits have been considered for compensation, operation of the varicap at zero bias or even a positive bias has not been considered, since it is difficult to generate a voltage very close to zero and have flexibility in choosing the voltage divider components.

To generate a zero bias with a voltage divider either Z_1 has to approach infinity or Z_2 has to be zero. Both of these cases impose requirements that are too extreme on the components. To eliminate these requirements a bridge circuit as shown in Figure 3.1.7 was tried, where diode D_1 is a varicap, $R_{c1} = R_{c2}$ and are isolating resistors; Z_1, Z_2, Z_3 and Z_4 are variable bridge variable resistances.



BRIDGE COMPENSATION NETWORK
Figure 3.1.7

The varicap can be biased slightly positive, and negative to values approaching B+. When biased in the forward range the voltage that can be applied to the varicap is limited because the diode begins conducting heavily at relatively small forward bias voltages. Although the forward voltage of the diode is limited by the diodes forward characteristics, the impedance exhibited by the diode will vary quite appreciably. This will enable the varicap to be used for compensation when biased slightly in the forward direction.

The following analysis of the bridge compensation networks was done using the circuit shown in Figure 3.1.7.

$R_t = Z_t = 2R_c + R_D$ where R_D is the varicap DC resistance. Equations 12 through 23 indicate the derivation of Equations 24 and 25. Equations 24 and 25 are the equations for the diode current and voltage as a function of the circuit parameters and the diode DC resistance.

$$12)\quad 0 = i_a\,(Z_1 + Z_2 + Z_T) + i_b\,(Z_T) + iZ_1$$

$$13)\quad 0 = i_a\,(Z_T) + i_b\,(Z_3 + Z_4 + Z_T) - iZ_4$$

$$14)\quad E = i_a\,Z_1 - i_b\,Z_4 + i\,(Z_1 + Z_4)$$

$$15)\quad i = -i_a\left(1 + \frac{Z_2}{Z_1} + \frac{Z_T}{Z_1}\right) - \frac{i_b Z_T}{Z_1}$$

$$16)\quad i_a = \frac{-\,i_b\left(Z_3 + Z_4 + Z_T + \frac{Z_4\,Z_T}{Z_1}\right)}{Z_T + \frac{Z_4}{Z_1}\left(Z_1 + Z_2 + Z_T\right)}$$

$$17)\quad E = i_a\left(Z_1 - Z_1 - Z_4 - Z_2 - \frac{Z_2 Z_4}{Z_1} - Z_T - \frac{Z_4 Z_T}{Z_1}\right) - i_b\left(Z_4 + Z_T + \frac{Z_4 Z_T}{Z_1}\right)$$

$$18)\quad E = \frac{i_b\left(Z_3 + Z_4 + Z_T + \frac{Z_4 Z_T}{Z_1}\right)\left(Z_4 + Z_2 + \frac{Z_2 Z_4}{Z_1} + Z_T + \frac{Z_4 Z_T}{Z_1}\right)}{Z_T + \frac{Z_4}{Z_1}\left(Z_1 + Z_2 + Z_T\right)} - i_b\left(Z_4 + Z_T + \frac{Z_4 Z_T}{Z_1}\right)$$

$$19)\ E = \frac{i_b(Z_1Z_3Z_4+Z_1Z_2Z_3+Z_2Z_3Z_4+Z_1Z_3Z_T+Z_3Z_4Z_T+Z_1Z_2Z_4+Z_1Z_2Z_T+Z_2Z_4Z_T)}{Z_1Z_T + Z_4Z_1 + Z_4Z_2 + Z_4Z_T}$$

$$20)\ i_b = \frac{E\ (Z_1Z_T + Z_1Z_4 + Z_2Z_4 + Z_4Z_T)}{(Z_1Z_3)(Z_4+Z_T+Z_2) + (Z_2Z_4)(Z_3+Z_T+Z_1) + Z_T(Z_1Z_2 + Z_3Z_4)}$$

Therefore:

$$21)\ i_a = -i_b\ \left(\frac{Z_1Z_3 + Z_1Z_4 + Z_1Z_T + Z_4Z_T}{Z_1Z_T + Z_1Z_4 + Z_2Z_4 + Z_4Z_T}\right)$$

$$22)\ i_a = \frac{-E\ (\ Z_1Z_3 + Z_1Z_4 + Z_1Z_T + Z_4Z_T)}{Z_1Z_3\ (Z_2+Z_4+Z_T) + Z_2Z_4\ (Z_1+Z_3+Z_T) + Z_T\ (Z_1Z_2+Z_3Z_4)}$$

$$23)\ i_D = i_a + i_b$$

$$24)\ i_D = \frac{E\ (Z_2Z_4 - Z_1Z_3)}{Z_1Z_3\ (Z_2+Z_4+Z_T) + Z_2Z_4\ (Z_1+Z_3+Z_T) + Z_T\ (Z_1Z_2+Z_3Z_4)}$$

$$25)\ V_D = \frac{R_D\ (Z_2Z_4 - Z_1Z_3)E}{Z_1Z_3\ (Z_2+Z_4+Z_T) + Z_2Z_4\ (Z_1+Z_3+Z_T) + Z_T\ (Z_1Z_2+Z_3Z_4)}$$

Equations 24 and 25 express the diode current and voltage as a function of the general parameters of the circuit. R_t is composed of the decoupling resistors R_c in series with the diode resistance R_D. In the case where the diode is reverse biased, R_D can be assumed to be infinite. Equations 24 and 25 then become,

$$26)\ i_D \doteq 0$$

27) $$V_D = \frac{(Z_2Z_4 - Z_1Z_3)E}{Z_1Z_3+Z_2Z_4+Z_1Z_2+Z_3Z_4}$$

If the diode is conducting, R_D approaches zero. Then Equations 28 and 29 can replace Equations 24 and 25.

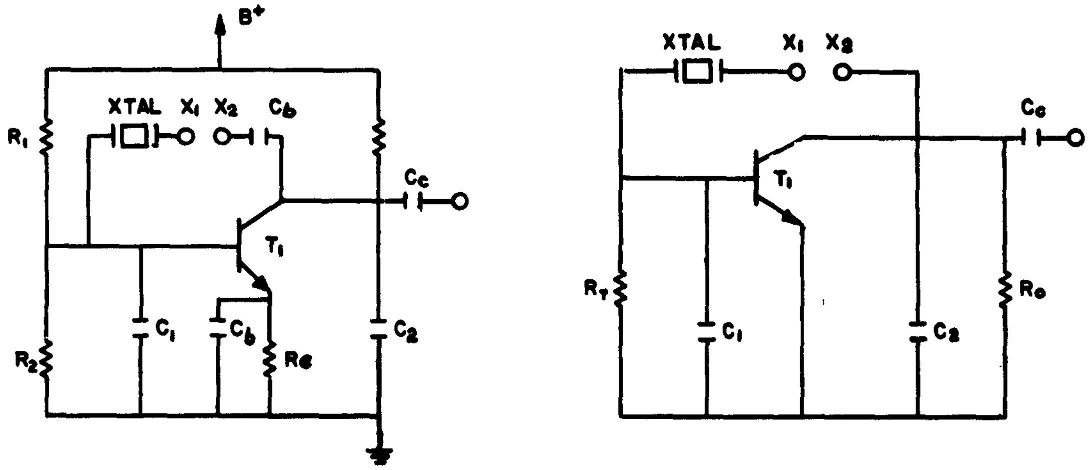
28) $$i_D = \frac{E(Z_2Z_4 - Z_1Z_3)}{Z_1Z_3(Z_2+Z_4+2R_c) + Z_2Z_4(Z_1+Z_3+2R_c) + 2R_c(Z_1Z_2+Z_3Z_4)}$$

29) $$V_D = 0$$

From Equation 25 it can be seen that if $Z_2Z_4 = Z_1Z_3$, then $V_D = 0$. This relationship is true for any magnitude of Z_1, Z_2, Z_3 and Z_4. To obtain zero bias with the bridge it is not necessary to approach 0 or infinity with any of the compensating resistances.

In Equations 24 and 25, R_t is composed partially of the diode resistance, R_D. Therefore, the resistance, R_t, is a function of V_o due to the diodes characteristics. If an equation can be written relating Z_D to i_D or V_D and if R_D can be expressed in terms of i_D or V_D, then the complete relationship between Z_D and i_D can be written in terms of the DC circuit parameters. This can be done to a very good approximation, but is not necessary for all practical purposes.

The oscillator configuration that is used for conducting tests and for compensation has been examined to optimize the parameter values. Figure 3.1.8(a) is the basic oscillator schematic that is being used. R_1, R_2, R_e and R_c are the transistor bias resistors. C_1 and C_2 are part of the oscillator network and form part of the crystal load impedance. Terminals X_1 and X_2 are the points of connection of the varicap or compensation network.



SCHEMATIC
(a)

AC EQUIVALENT CIRCUIT
(b)

BASIC OSCILLATOR CONFIGURATION
Figure 3.1.8

The ratio of C_1 to C_2 and the magnitude of C_1 and C_2 affects the range of the compensation circuit and the stability of the oscillator. By simply examining the equivalent a-c circuit for the oscillator shown in Figure 3.1.8(b), it can be seen that if C_1 and C_2 are increased, the effect of C_x will become greater. Stray capacitance will be damped out by the increase in C_1 and C_2, which results in increased circuit stability.

The effect of using various types of varicaps and paralleling varicaps with capacitors to obtain different characteristics was investigated. The frequency of the oscillator was set to the crystal frequency corresponding to a load capacity of 32 pfd when four volts was applied across the varicap. Curves #1 through #4 in Figure 3.1.9 indicate the effect on the pullability of the varicaps as a function of varicap type and parallel capacitance combination.

Oscillators used in the work performed during the first quarter in general had inductors placed in series with the crystal to operate the crystal at series resonance. Curves obtained for the frequency versus tempera-

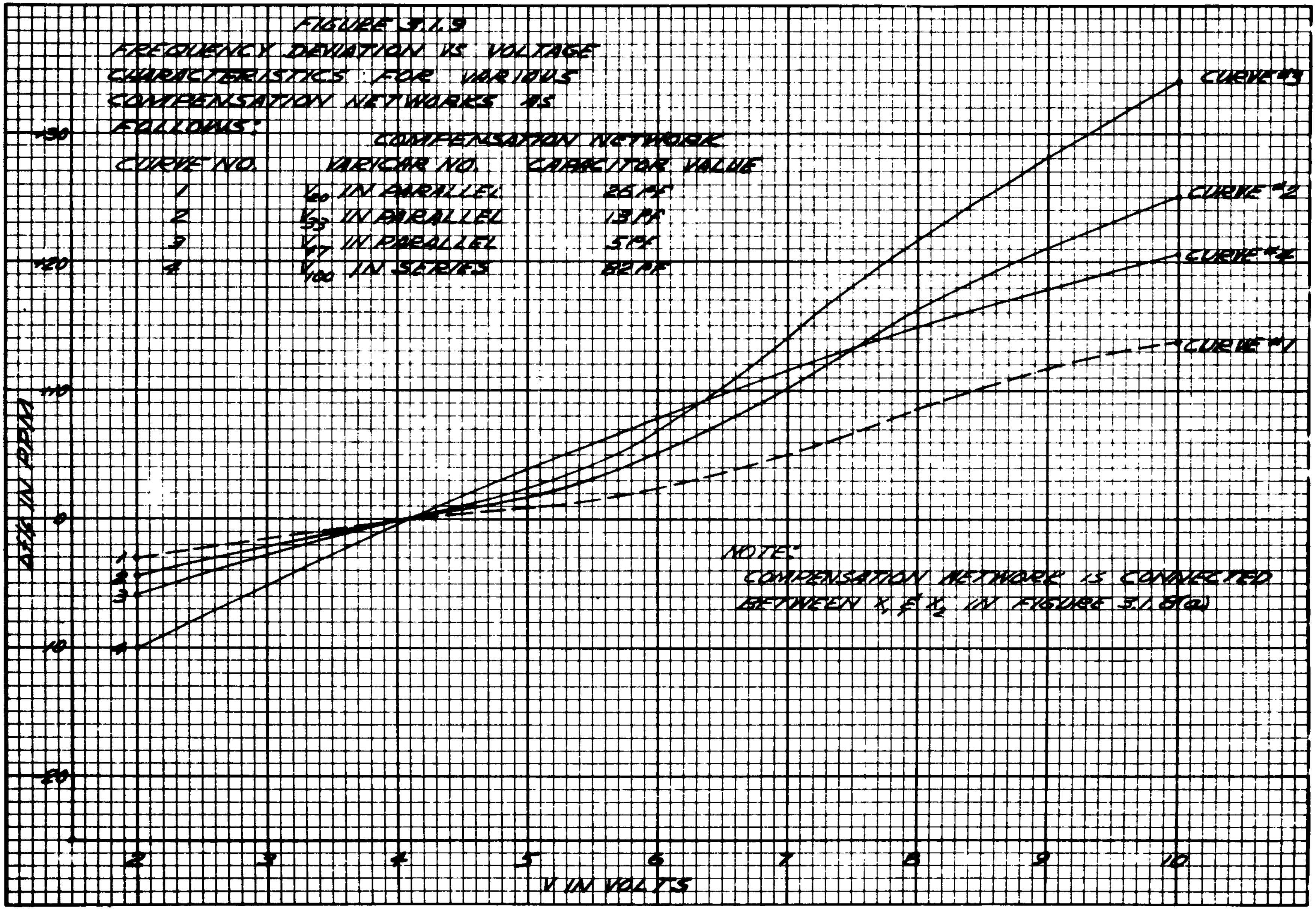


FIGURE 3.1.9
FREQUENCY DEVIATION VS VOLTAGE
CHARACTERISTICS FOR VARIOUS
COMPENSATION NETWORKS AS
FOLLOWS:
COMPENSATION NETWORK
CURVE NO. VARICAP NO. CAPACITOR VALUE
1 V20 IN PARALLEL 26 PF
2 V33 IN PARALLEL 13 PF
3 V47 IN PARALLEL 5 PF
4 V100 IN SERIES 82 PF
CURVE #3
CURVE #2
CURVE #4
CURVE #1
NOTE:
COMPENSATION NETWORK IS CONNECTED
BETWEEN X1 & X2 IN FIGURE 3.1.8(a)
+30
+20
+10
0
10
20
DEV. IN PPM
2
3
4
5
6
7
8
9
10
V IN VOLTS

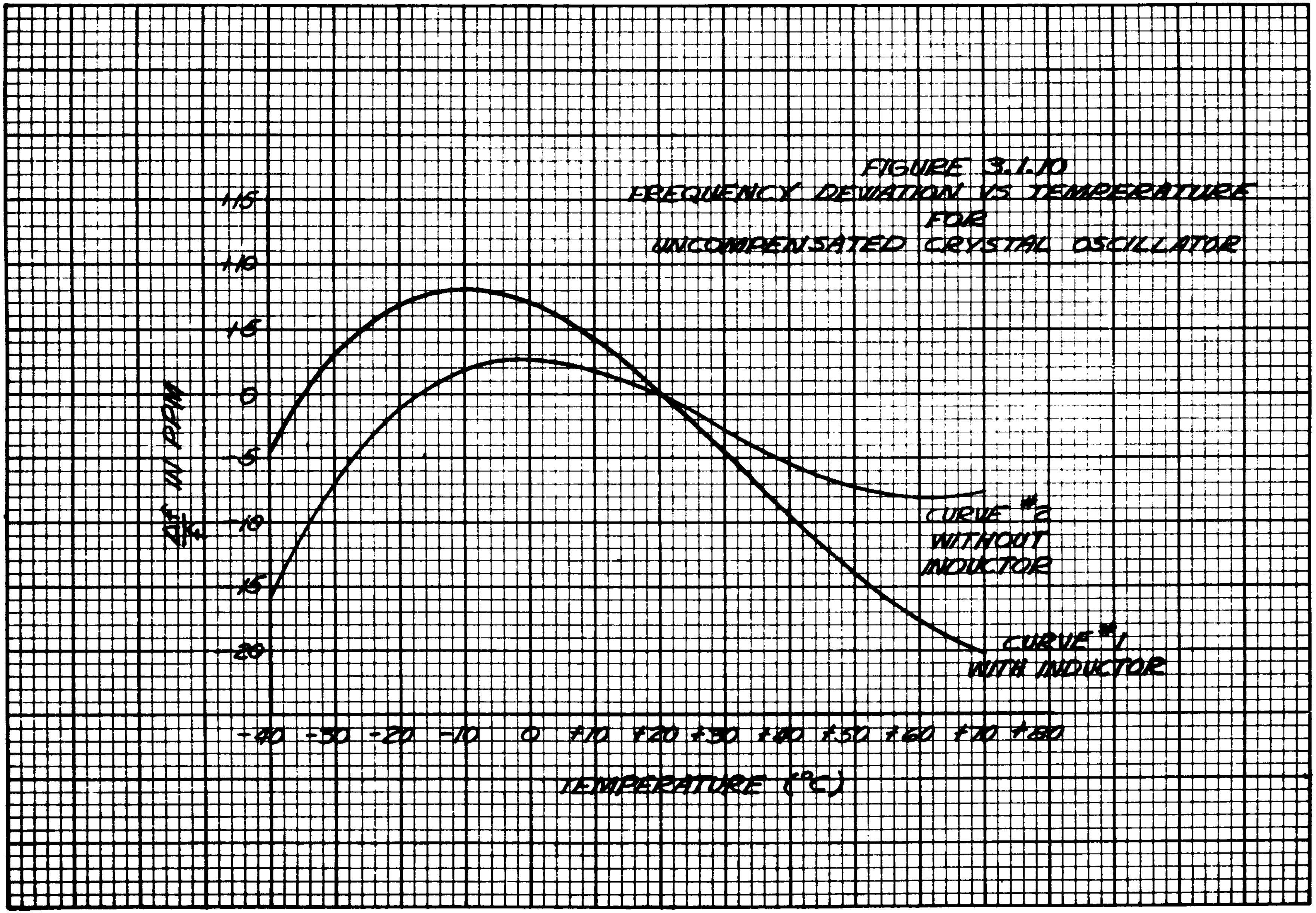
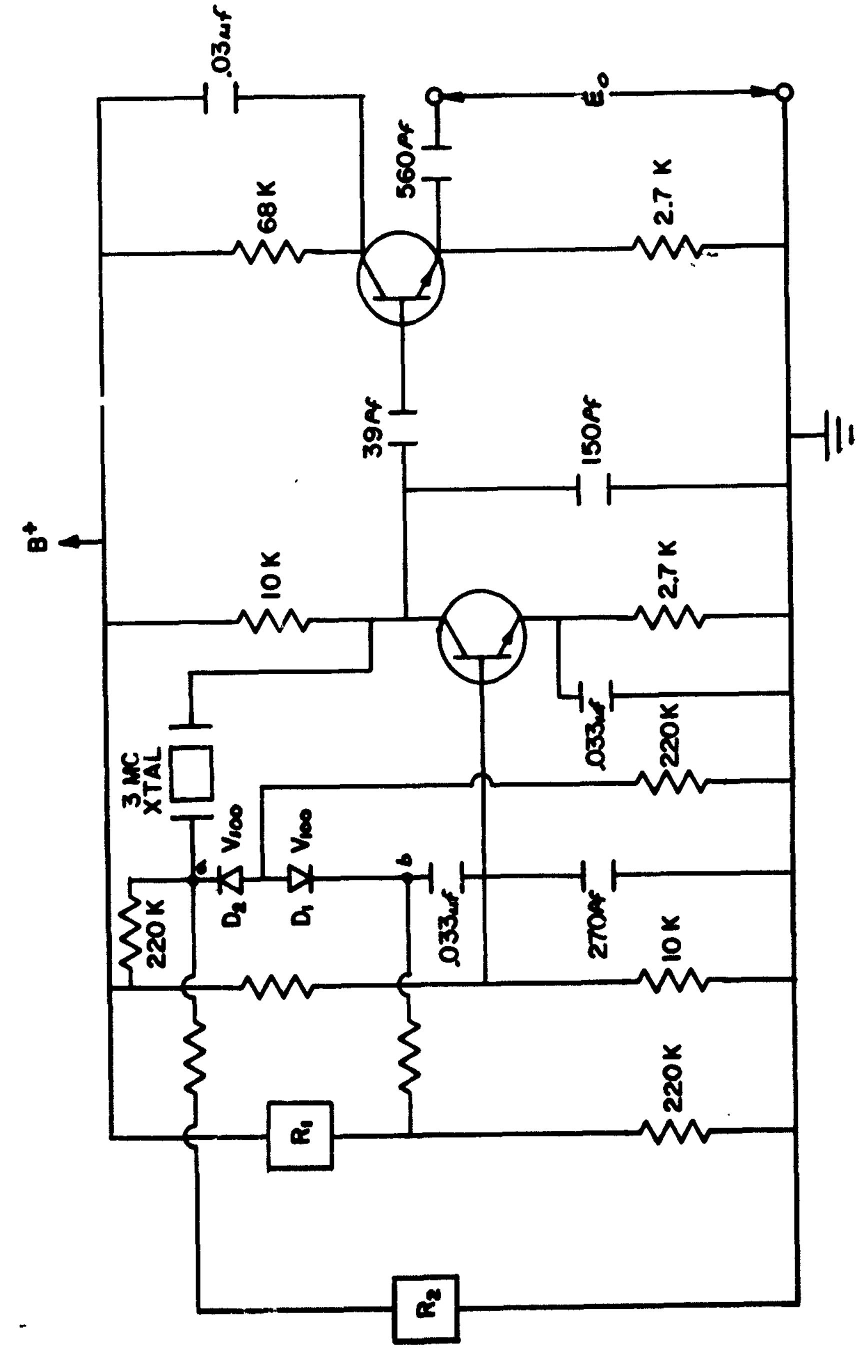


FIGURE 3.1.10
FREQUENCY DEVIATION VS TEMPERATURE
FOR
UNCOMPENSATED CRYSTAL OSCILLATOR

ture characteristics of a number of oscillators were not consistant with the crystal curves. To determine what caused this, a number of tests were performed, one of which was checking the frequency temperature characteristics of oscillator with and without an inductor. Figure 3.1.10 indicates the effect of one inductor. This particular inductor had a very large temperature coefficient which was not typical, but indicated that the error in the frequency-temperature characteristics was probably due to the temperature coefficient of the series inductors.

A number of test circuits were built to test the characteristics of the two varicap compensation methods. The first test was directed at finding whether or not changing one of the compensating resistances affected the characteristics of the $\Delta f/f$ versus resistance of the other compensating networks.

The oscillator used for the tests is shown in Figure 3.1.11. R_1 is the control resistance for varicap, D_1 and D_2 are the control resistance for varicap D_2. Figure 3.1.12 shows the effect of changing R_2 on the $\Delta f/f$ versus R_1 characteristics of the compensation circuit. The two curves indicate that the effect is negligible, because the frequency was only recorded to an accuracy of $\pm$ 3 parts in 10^7 and the maximum deviation shown in Figure 3.1.12 is 1 PPM. Figure 3.1.13 shows the effect of changing R_1 on the $\Delta f/f$ versus R_2 characteristics of the oscillator. The maximum deviation is approximately 1.5 PPM. Under normal conditions R_1 will only vary slightly when R_1 is being used for compensation. The variation of R_2 in Figure 3.1.13 and R_1 in Figure 3.1.12 is many times what will normally be expected; therefore, the error in the compensation curve will be considerably less than the total deviation shown in Figure 3.1.12 and 3.1.13.



TWO VARICAP COMPENSATED OSCILLATOR
FIGURE 3.1.11

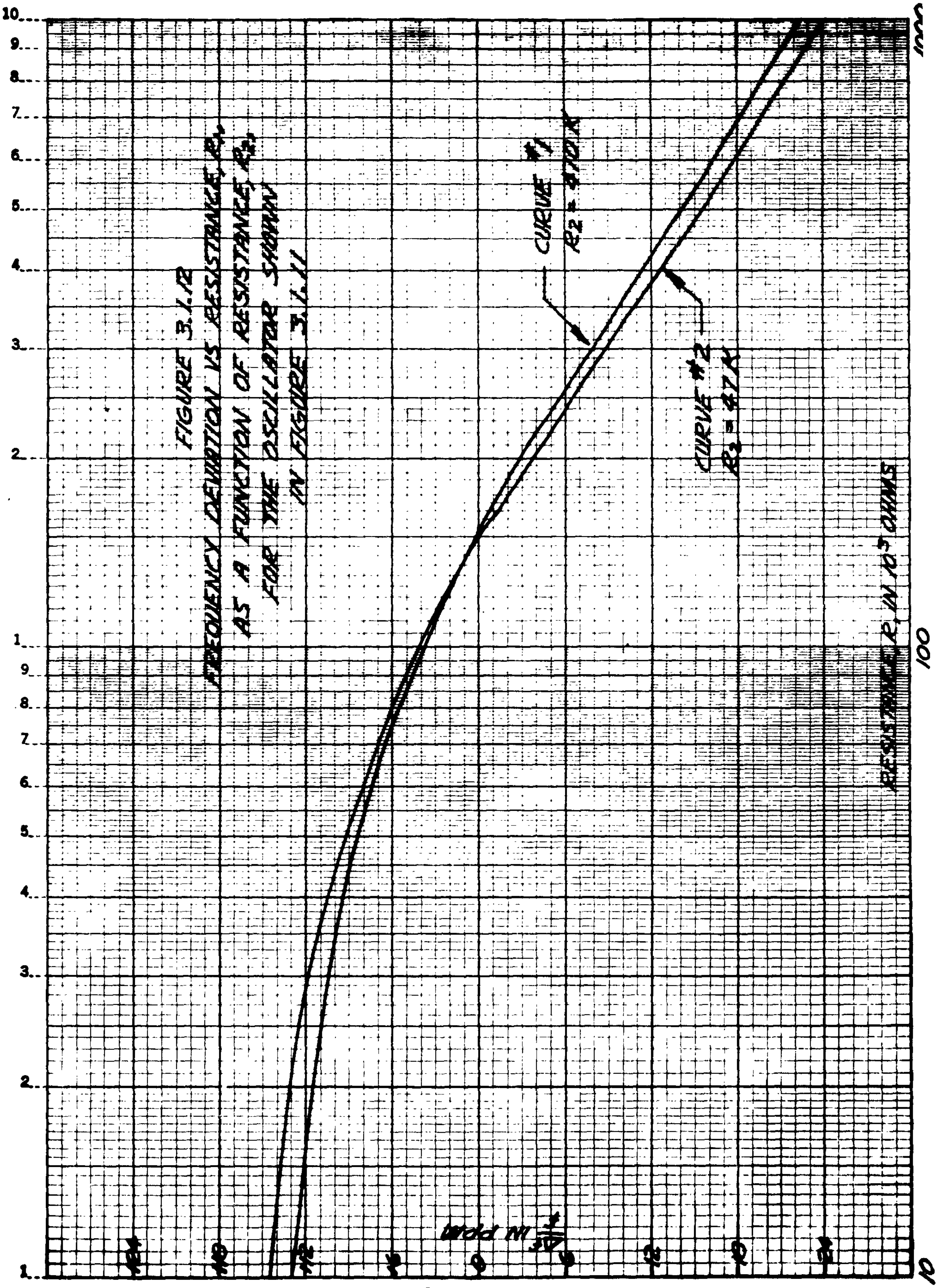


FIGURE 3.1.12
FREQUENCY DEVIATION VS RESISTANCE, R_1,
AS A FUNCTION OF RESISTANCE, R_2,
FOR THE OSCILLATOR SHOWN
IN FIGURE 3.1.11

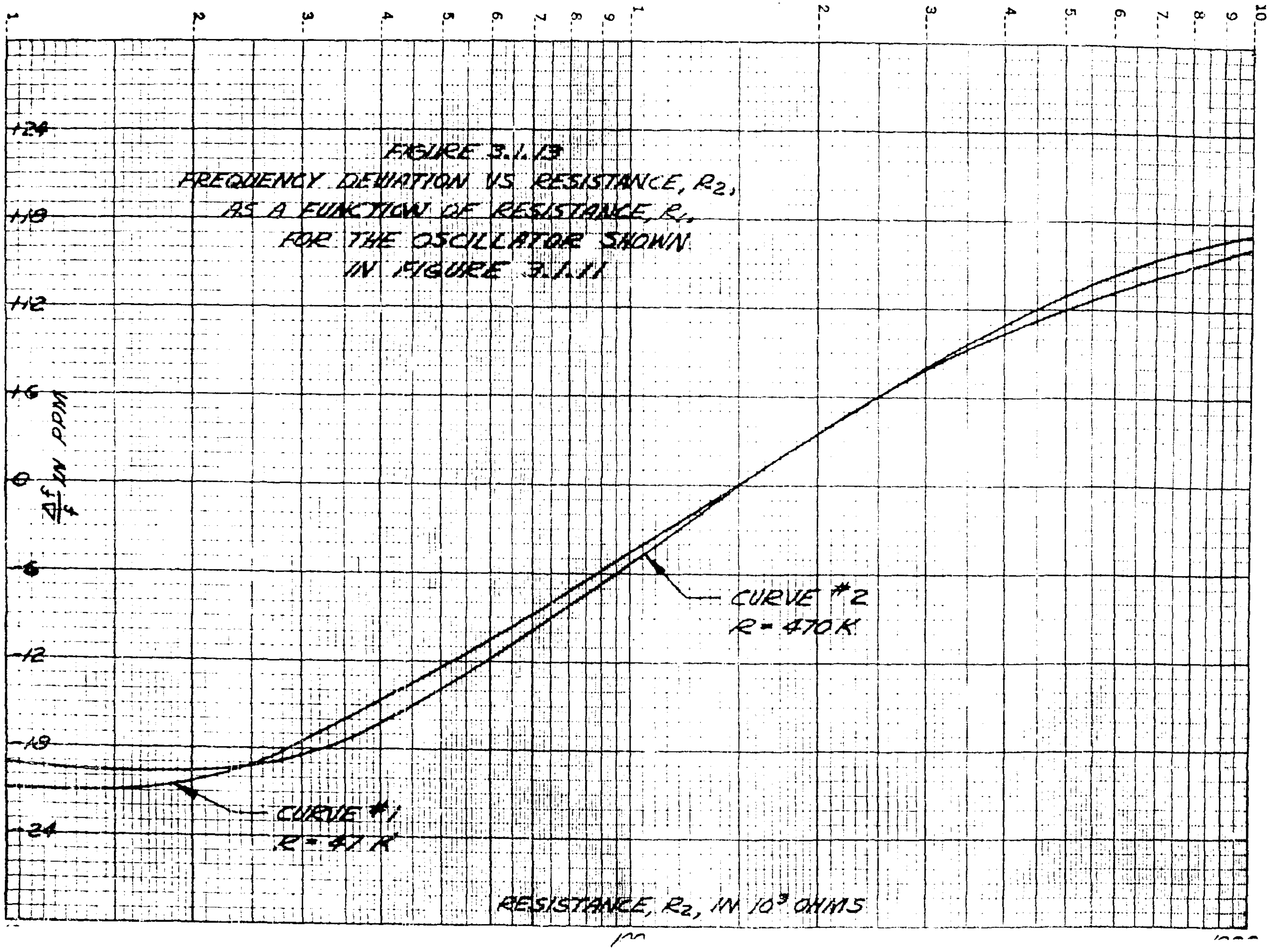


FIGURE 3.1.13
FREQUENCY DEVIATION VS RESISTANCE, R_2,
AS A FUNCTION OF RESISTANCE, R_1,
FOR THE OSCILLATOR SHOWN
IN FIGURE 3.1.11

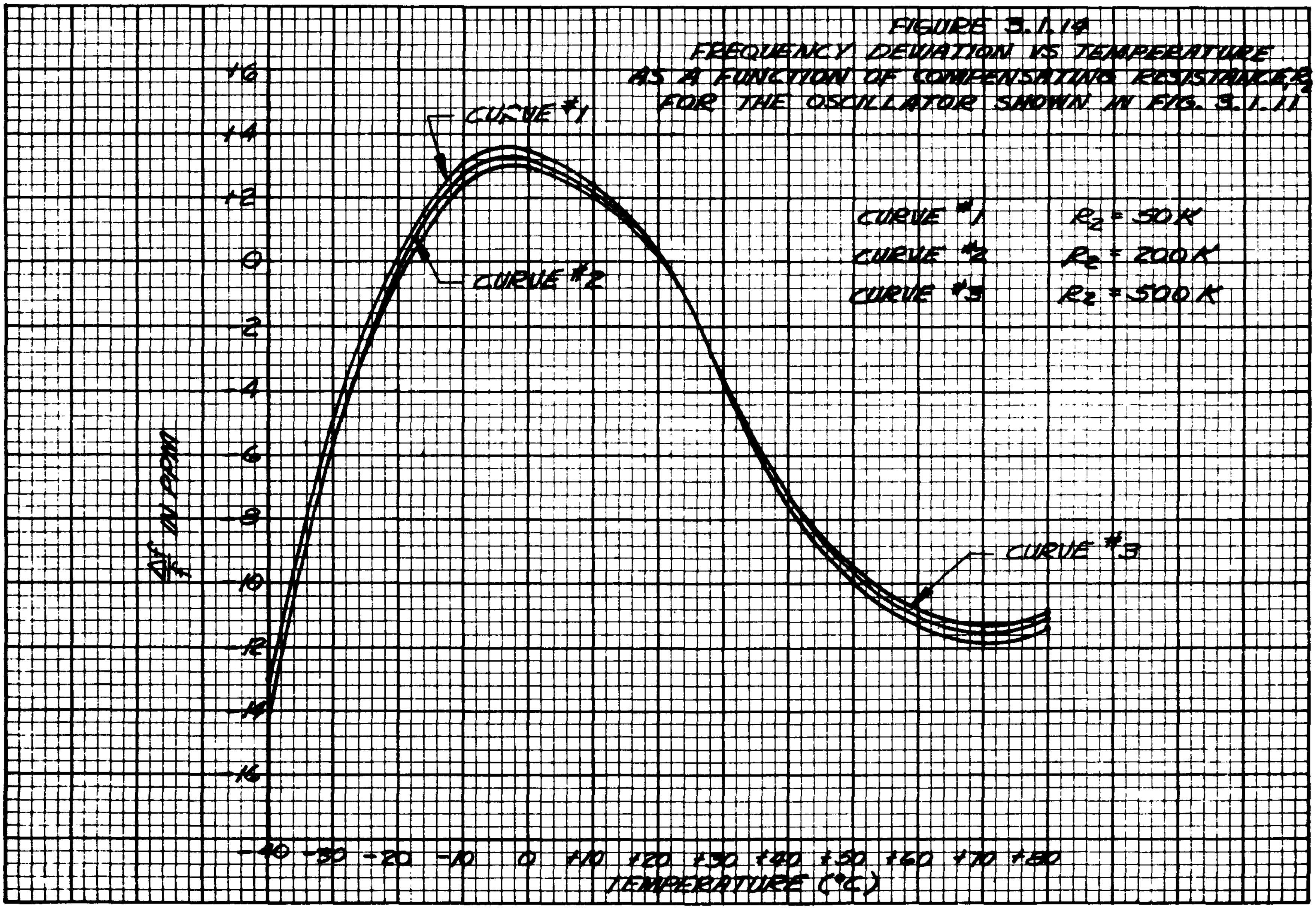
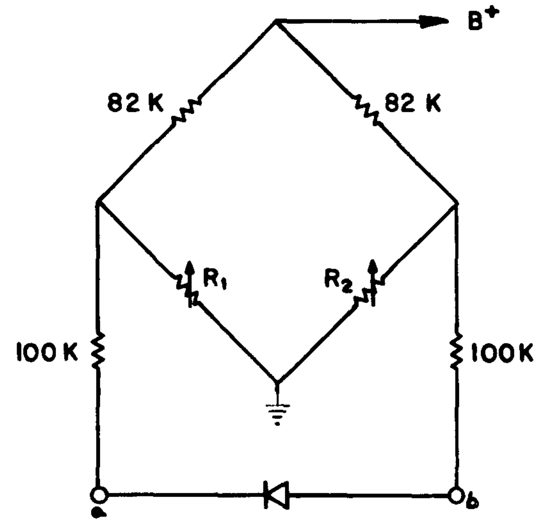


FIGURE 3.1.14
FREQUENCY DEVIATION VS TEMPERATURE
AS A FUNCTION OF COMPENSATING RESISTANCE R2
FOR THE OSCILLATOR SHOWN IN FIG. 3.1.11
CURVE #1 R2 = 50K
CURVE #2 R2 = 200K
CURVE #3 R2 = 500K
CURVE #1
CURVE #2
CURVE #3
Δf/f IN PPM
+6
+4
+2
0
-2
-4
-6
-8
-10
-12
-14
-16
-40 -30 -20 -10 0 +10 +20 +30 +40 +50 +60 +70 +80
TEMPERATURE (°C)

The temperature effect of the varicap with various biasing resistances is another area where a problem may be present. Figure 3.1.14 is a curve of $\Delta f/f$ versus temperature for the oscillator for various values of R_2. The effect of the compensation network can be assumed negligible, because the errors observed were within the accuracy limitations of the frequency measurements. A large number of varicaps were tried in this same circuit and the results were all similar to those that are shown in Figures 3.1.12, 3.1.13, and 3.1.14.



TYPICAL BRIDGE CIRCUIT USED FOR COMPENSATION STUDIES
Figure 3.1.15

The test circuit shown in Figure 3.1.15 is the bridge circuit which was connected to points (a) and (b) in Figure 3.1.11 to obtain data on a varicap in a bridge circuit. Figure 3.1.16 shows the frequency characteristics of the oscillator as a function of the bridge resistances R_1 and R_2. In this case R_2 was varied while R_1 was set equal to 68 K and R_1 varied while R_2 was set equal to 500 K. The purpose for this can be seen if the curves are related to the changes required for R_1 and R_2 to compensate an AT cut crystal. R_2 will control the compensation network for temperatures above the lower

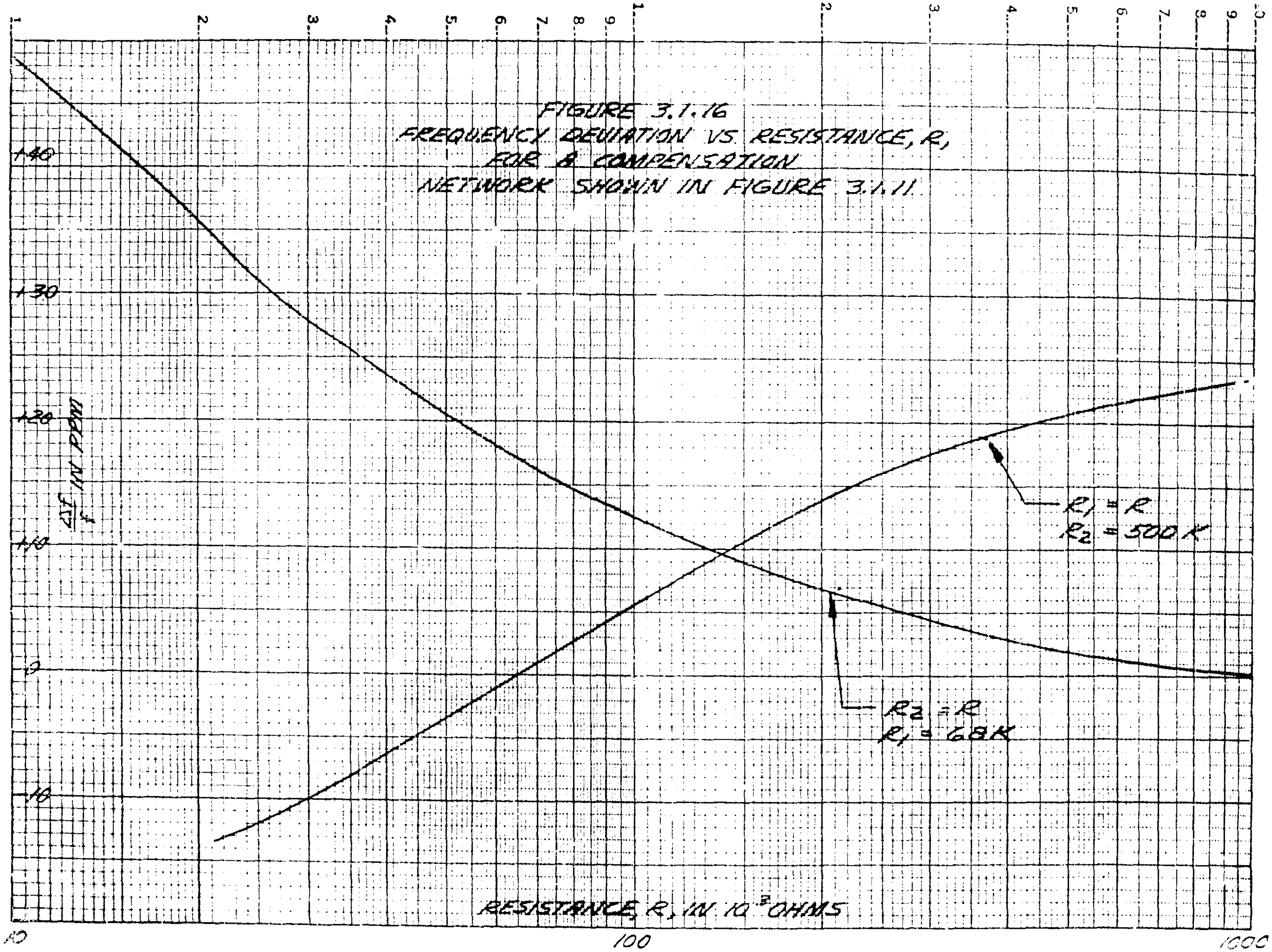


FIGURE 3.1.16
FREQUENCY DEVIATION VS RESISTANCE, R, FOR A COMPENSATION NETWORK SHOWN IN FIGURE 3.1.11
R1 = R
R2 = 500 K
R2 = R
R1 = 68K
Δf/f IN PPM
+40
+30
+20
+10
0
-10
RESISTANCE R, IN 10^3 OHMS
10
100
1000

turning point of the crystals characteristic frequency-temperature curve and R_1 will control the compensation network below the turning point. Thus, R_1 and R_2 will both be small at the highest temperature, then R_2 will increase and R_1 will remain constant as the temperature is decreased to the lower turning point, where R_1 will increase and R_2 held constant as the temperature is further reduced to a minimum value.

Figure 3.1.17 indicates the frequency versus resistance, R_1, as a function of R_2 characteristics of the oscillator using the network shown. As can be seen from the curves, the magnitude of R_2 has a very pronounced effect on the $\Delta f/f$ versus R_1 characteristics of the compensation network. When R_1 is small, R_2 has little effect on the slope of the $\Delta f/f$ versus R_1 curve, but as R_1 is increased, R_2 has a considerable effect on the characteristics. The reason for the effect of R_2 on the $\Delta f/f$ versus R_1 characteristics is due to the effect of forward biasing the varicap. When the varicap is reverse biased and slightly forward biased, the characteristics of the compensation network is uniform, but as the diode becomes more forward biased the diode's characteristics change appreciably as can be deduced from the curves in Figure 3.1.17.

Figure 3.1.18 is a graph that compares the voltage output versus resistance of a bridge circuit and a voltage divider. If all resistance values are held constant, then the bridge circuit voltage output goes from 0 to a maximum of B+/2 and the voltage divider output goes from 0 to a maximum of B+. But, the resistance in the voltage divider must vary from 0 to infinity, where the resistance in the bridge must only vary from some arbitrary value, R, to infinity.

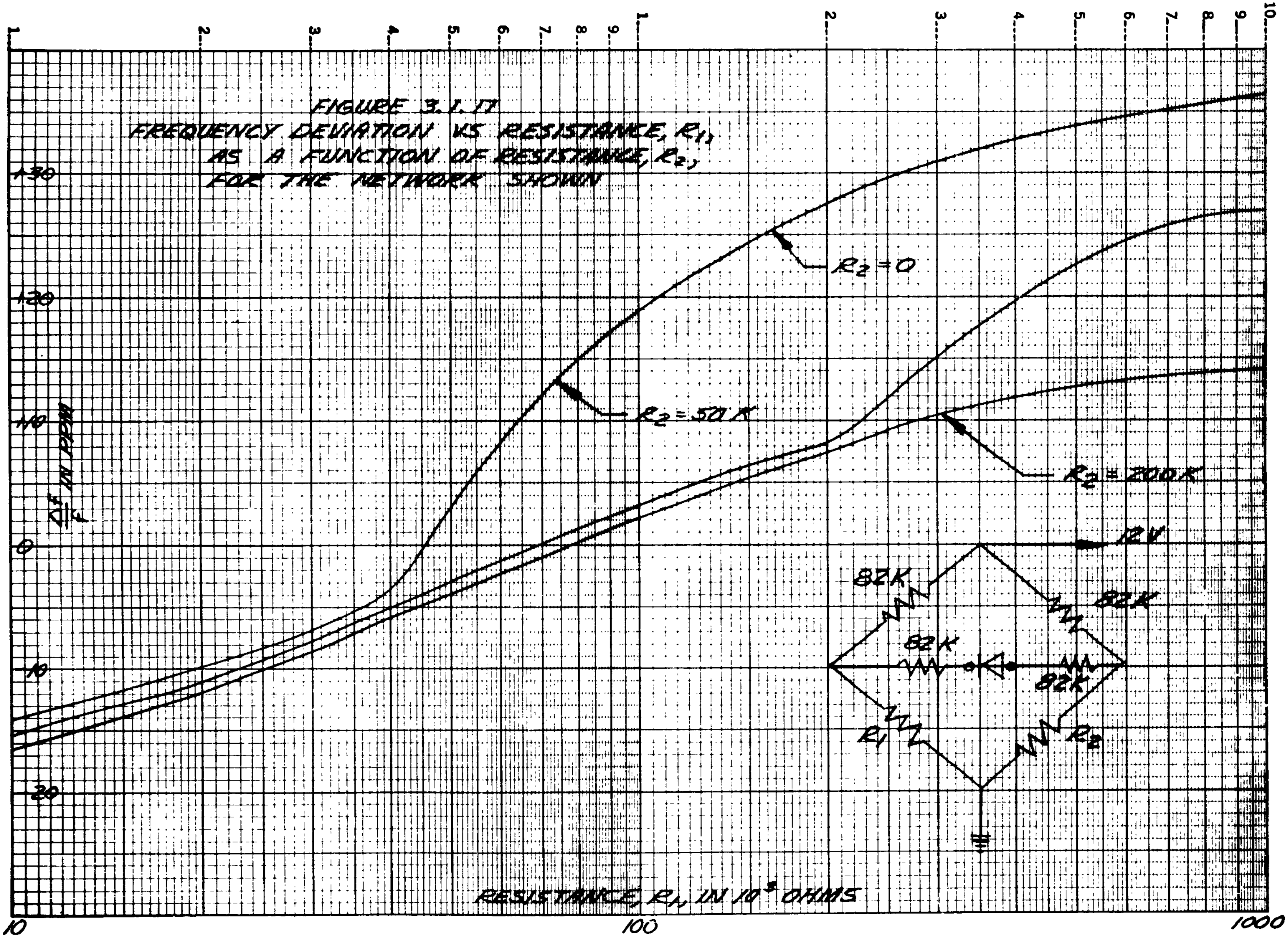
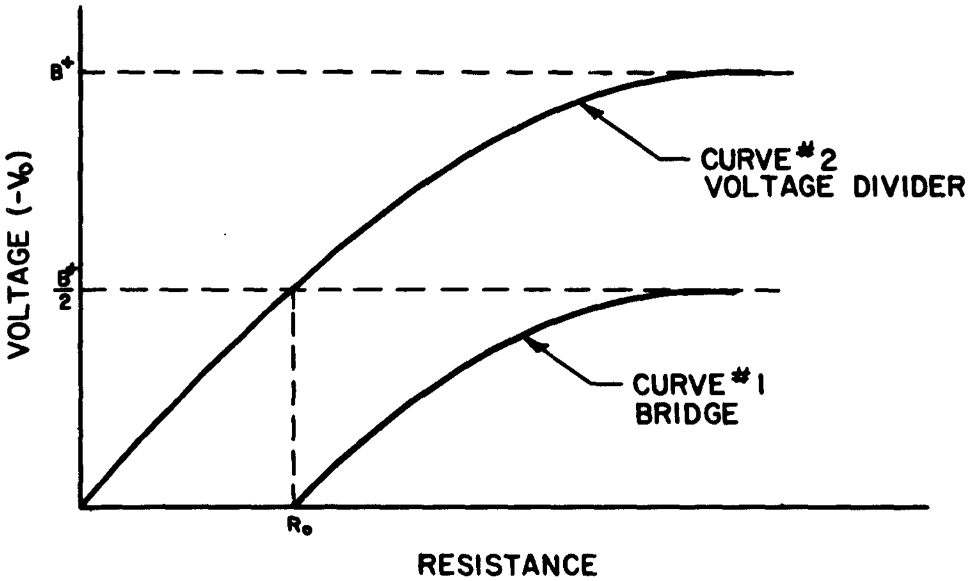


FIGURE 3.1.17
FREQUENCY DEVIATION VS RESISTANCE, R_1, AS A FUNCTION OF RESISTANCE, R_2, FOR THE NETWORK SHOWN



COMPARISON OF BRIDGE AND VOLTAGE DIVIDER
VOLTAGE OUTPUTS AS A FUNCTION OF RESISTANCE
Figure 3.1.18

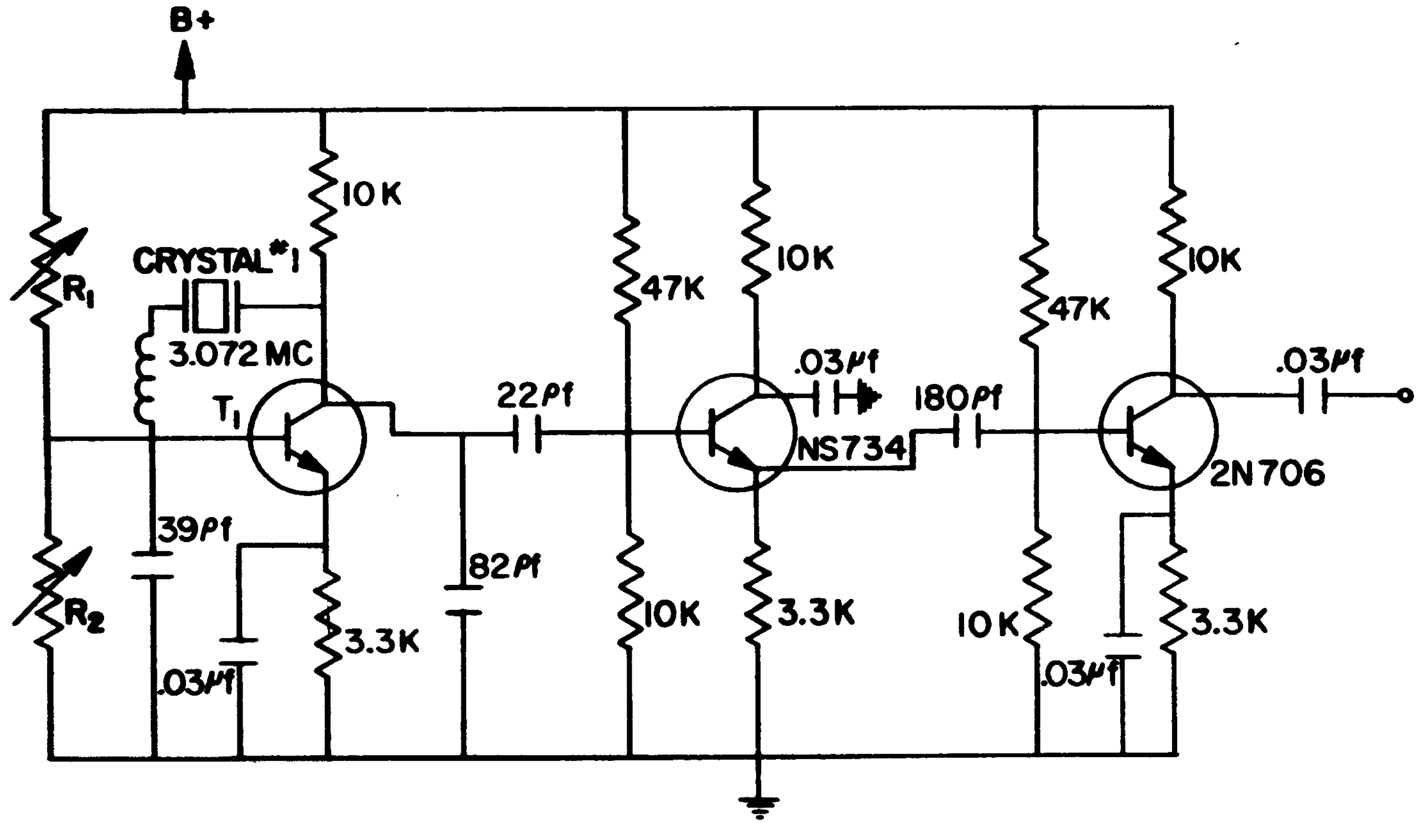
3.2 Transistor Method

The theory of the transistor method of compensation was presented in the First Quarterly Report and will not be discussed at length in this report. In the previous Quarterly Report is was shown that compensation could be achieved by using the collector to base junction capacitance of the transistor. The remaining questions to be answered about this method of compensation are (1) the degree of compensation that can be obtained using the transistor method, (2) the reproducibility of a compensation curve provided by using various transistors in a fixed oscillator and compensation network configuration, (3) the effect of temperature on the pullability curves, and (4) difficulty of synthesizing a required compensation network.

A series of tests were performed on a number of transistors in an effort to answer some of the above questions. The oscillator shown in Figure 3.2.1 was used for these tests, where all of the components remained the same except the transistor. A group of five transistors were tested in this circuit. The transistors used and their corresponding DC betas are listed below.

Table #1

	Type	Manufacturer	DC Beta
1.	2N697	Texas Instruments	53
2.	2N697	Texas Instruments	62
3.	2N697	Fairchild	64
4.	RT(5230)	Rheem Semiconductor	92
5.	RT(5230)	Rheem Semiconductor	91



SCHEMATIC OF OSCILLATOR USED FOR TRANSISTOR METHOD

FIGURE 3.2.1

R_1 and R_2 in Figure 3.2.1 are decade boxes in the test circuit and would be replaced by thermistor-resistor networks when the oscillator was to be compensated over temperature. If NTC thermistors are used for compensation, then R_1 and R_2 will be at their maximum values at the lowest ambient temperature and they will be at their minimum values at the highest ambient temperature. This dictates what part of the crystal $\Delta f/f$ versus temperature curve that R_1 and R_2 will control. In general, as R_1 decreases, the frequency decreases and as R_2 decreases the frequency increases. Therefore, if an AT cut crystal is to be compensated, R_1 must be used for temperature compensation from the lowest temperature to the lower turning point and R_2 must be used from the lower turning point to the upper turning point.

With this fact in mind, the pullability curves, $\Delta f/f$ versus R, were obtained by setting both R_1 and R_2 at their maximum values or the largest value at which they should be operated. R_1 was then decreased to its lowest value and the $\Delta f/f$ versus R_1 data was recorded. Then R_1 was left at its minimum value, while the $\Delta f/f$ versus R_2 data was recorded as R_2 was varied from its maximum to its minimum value. This in effect simulates the manner in which R_1 and R_2 would have to vary as the temperature changes from its lowest value to its maximum value. Figure 3.2.2 through 3.2.6 are the pullability curves of $\Delta f/f$ versus R_1 for the five transistors tested as a function of temperature. Figures 3.2.7 through 3.2.11 are the pullability curves of $\Delta f/f$ versus R_2 for the five transistors tested as a function of temperature.

Figure 3.2.12 and 3.2.13 compare the pullability at room temperature of the five transistors that were tested. As can be seen, Transistor #5 has the greatest change in frequency and Transistor #1 has the least change for a given change in resistance. The characteristics of the five transistors tested are all similar. The only difference in the curves is the slope or the

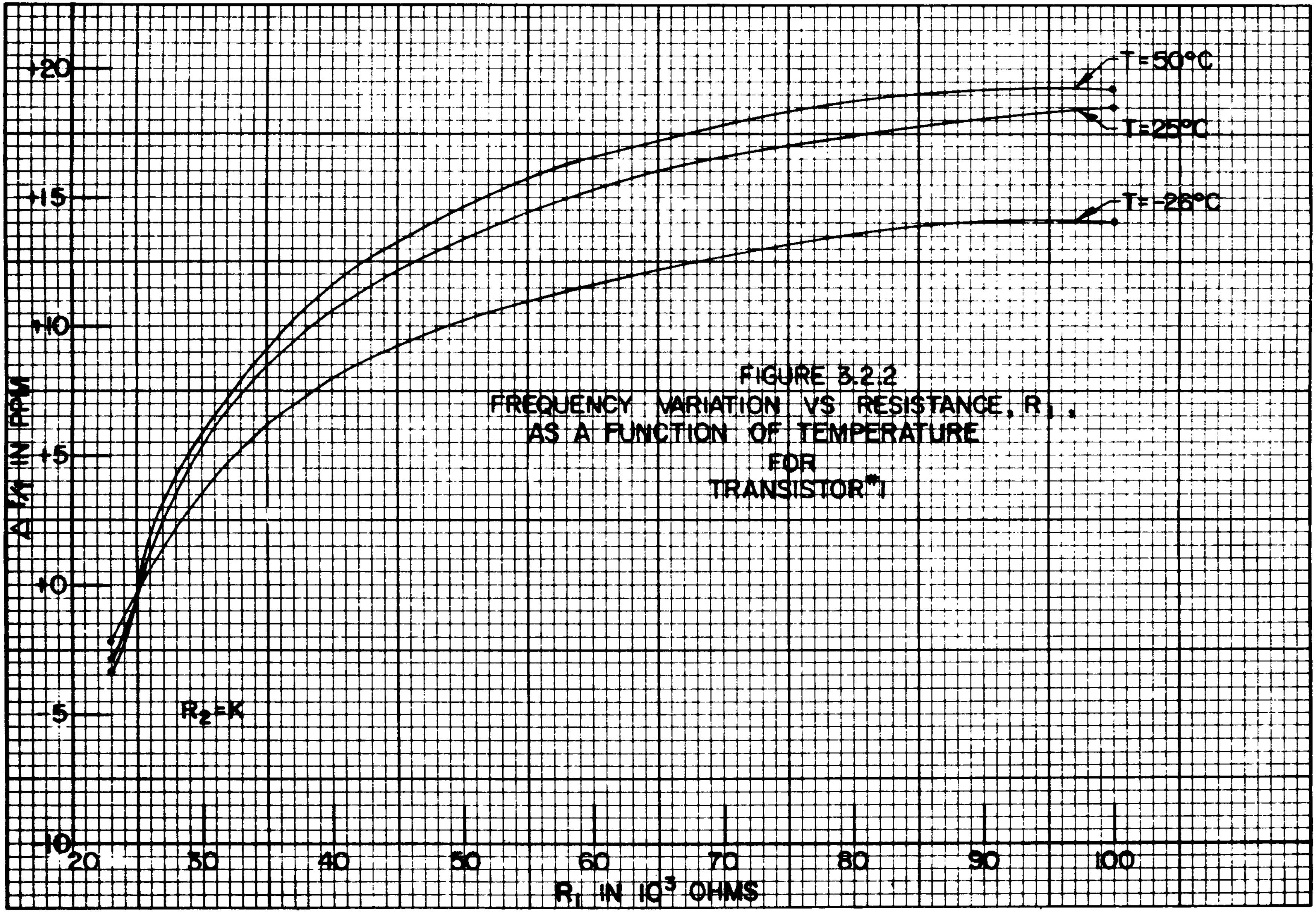


FIGURE 3.2.2
FREQUENCY VARIATION VS RESISTANCE, R_1, AS A FUNCTION OF TEMPERATURE FOR TRANSISTOR #1
T=50°C
T=25°C
T=-26°C
R_2=K
+20
+15
+10
+5
+0
-5
-10
20
30
40
50
60
70
80
90
100
$\Delta f/f$ IN PPM
R_1 IN 10^3 OHMS

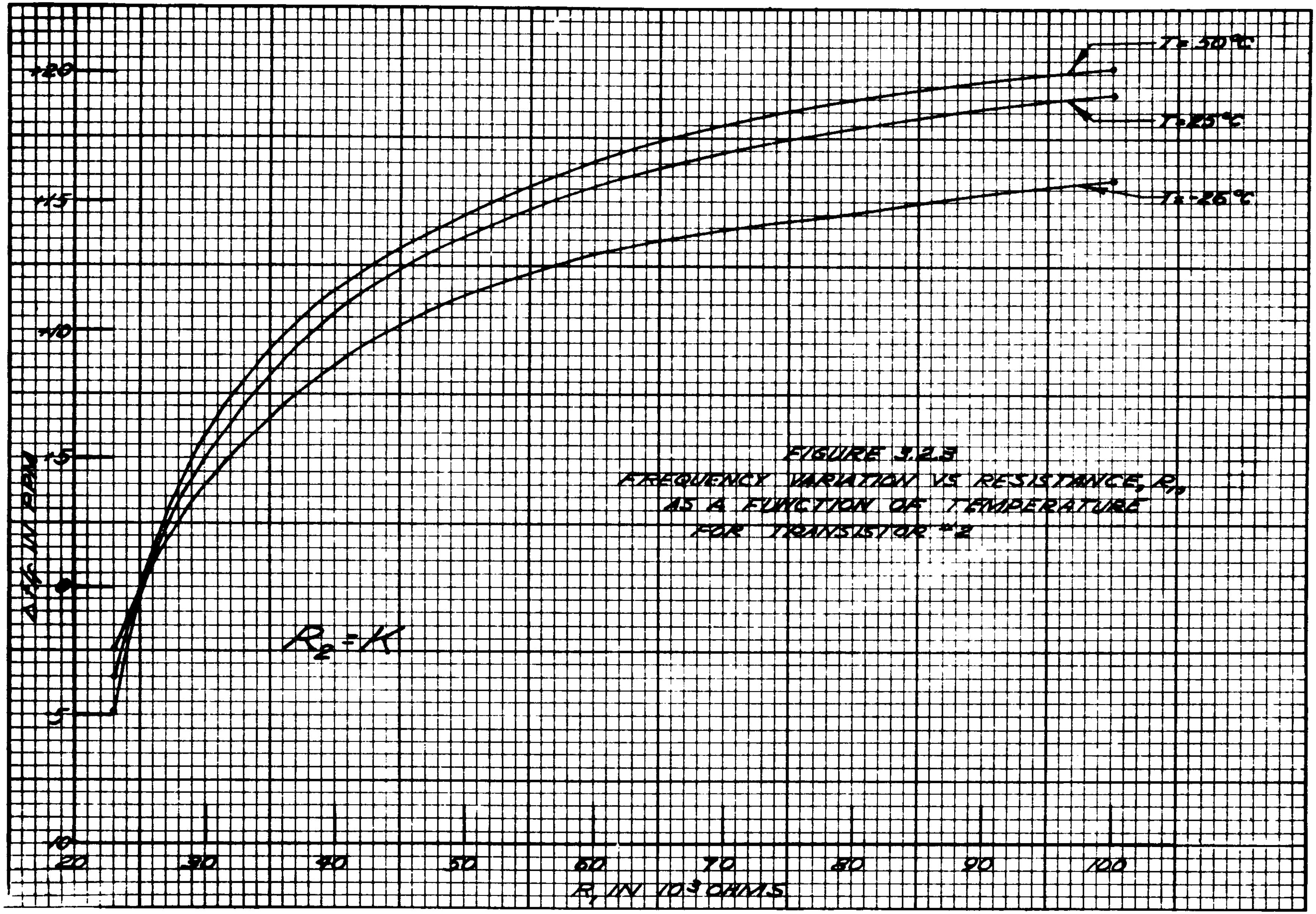


FIGURE 3.2.3
FREQUENCY VARIATION VS RESISTANCE, R_{11}
AS A FUNCTION OF TEMPERATURE
FOR TRANSISTOR #2

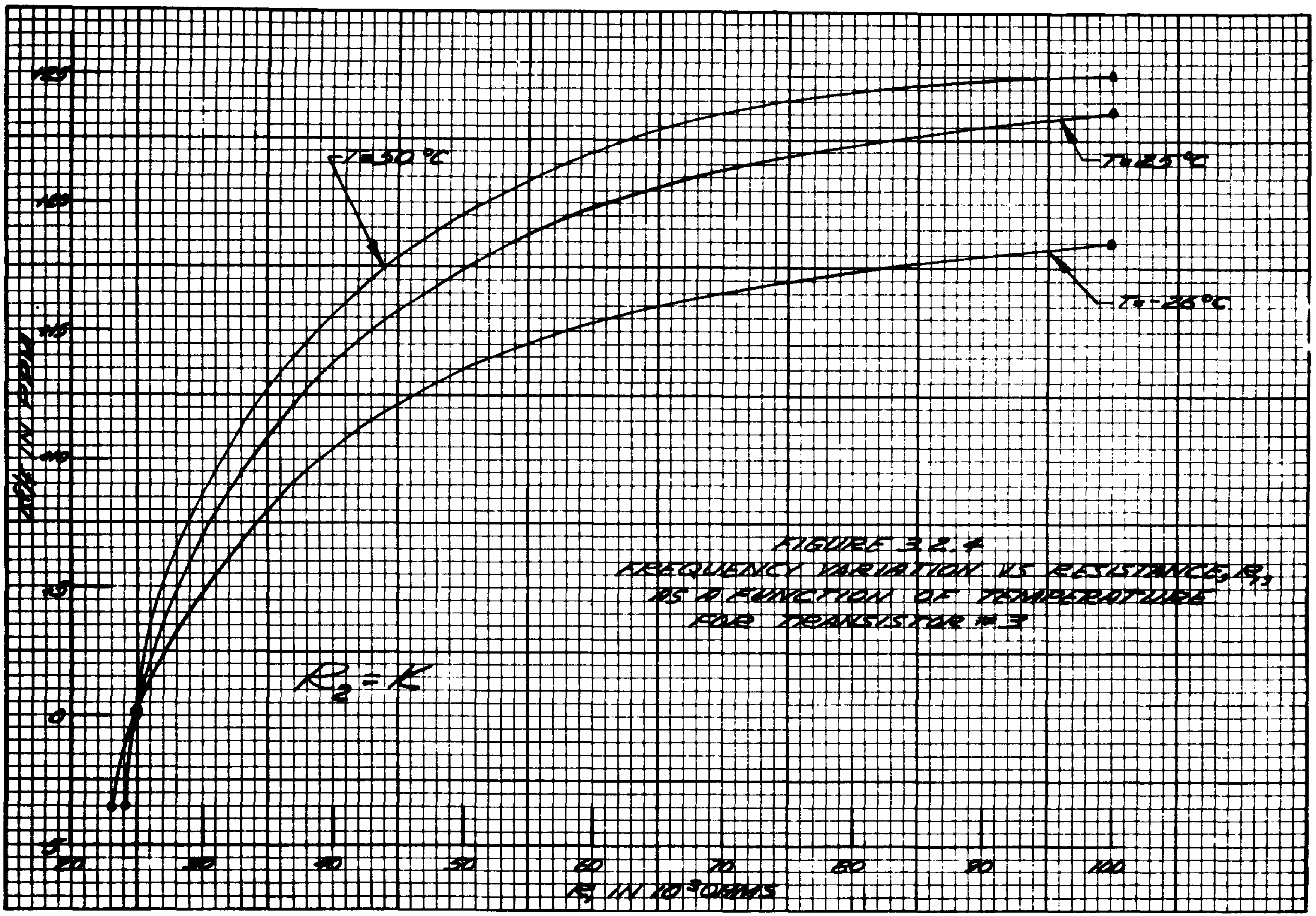


FIGURE 3.2.4
FREQUENCY VARIATION VS RESISTANCE, R_1
AS A FUNCTION OF TEMPERATURE
FOR TRANSISTOR #3

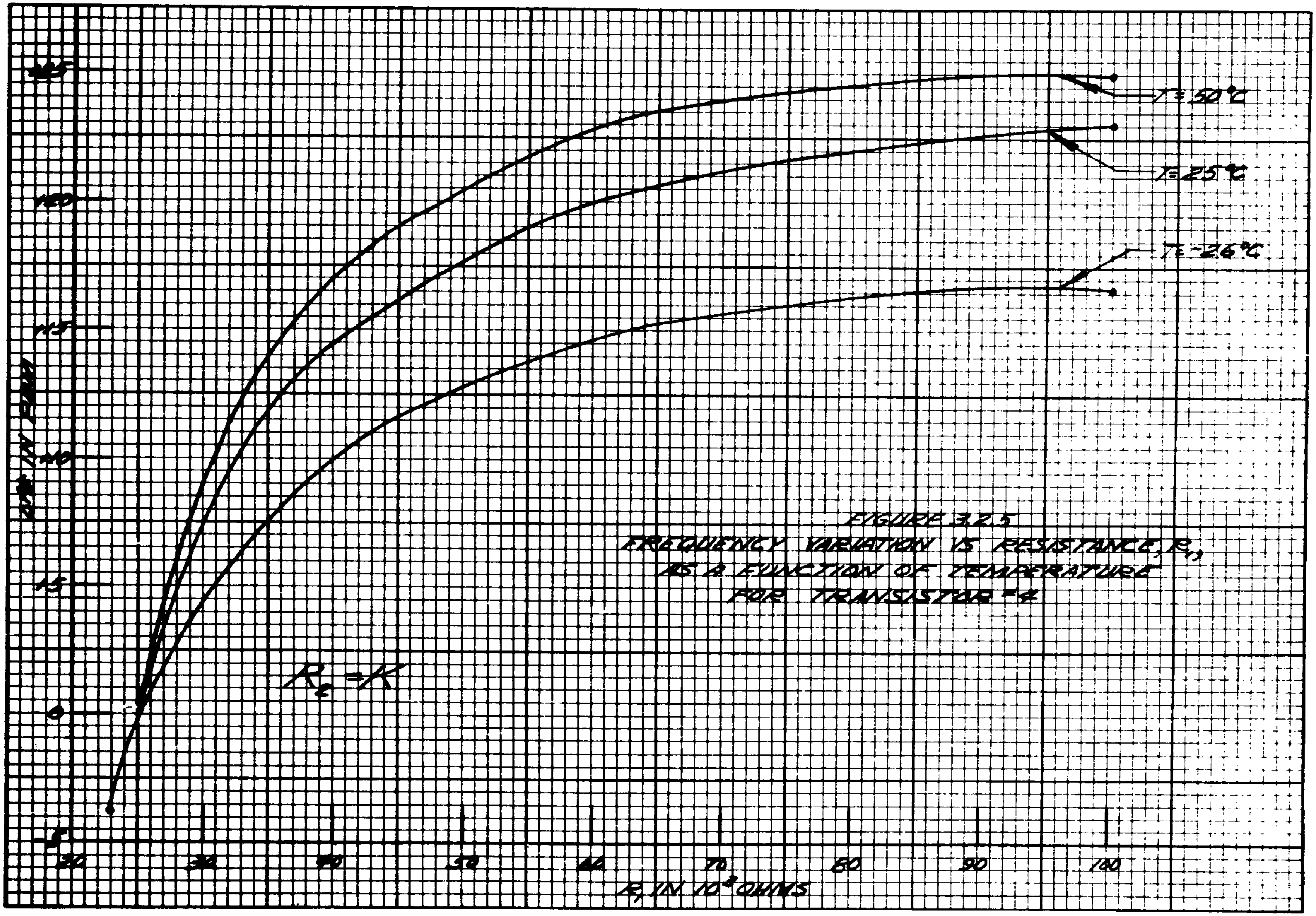


FIGURE 3.2.5
FREQUENCY VARIATION VS RESISTANCE, R_1,
AS A FUNCTION OF TEMPERATURE
FOR TRANSISTOR #4

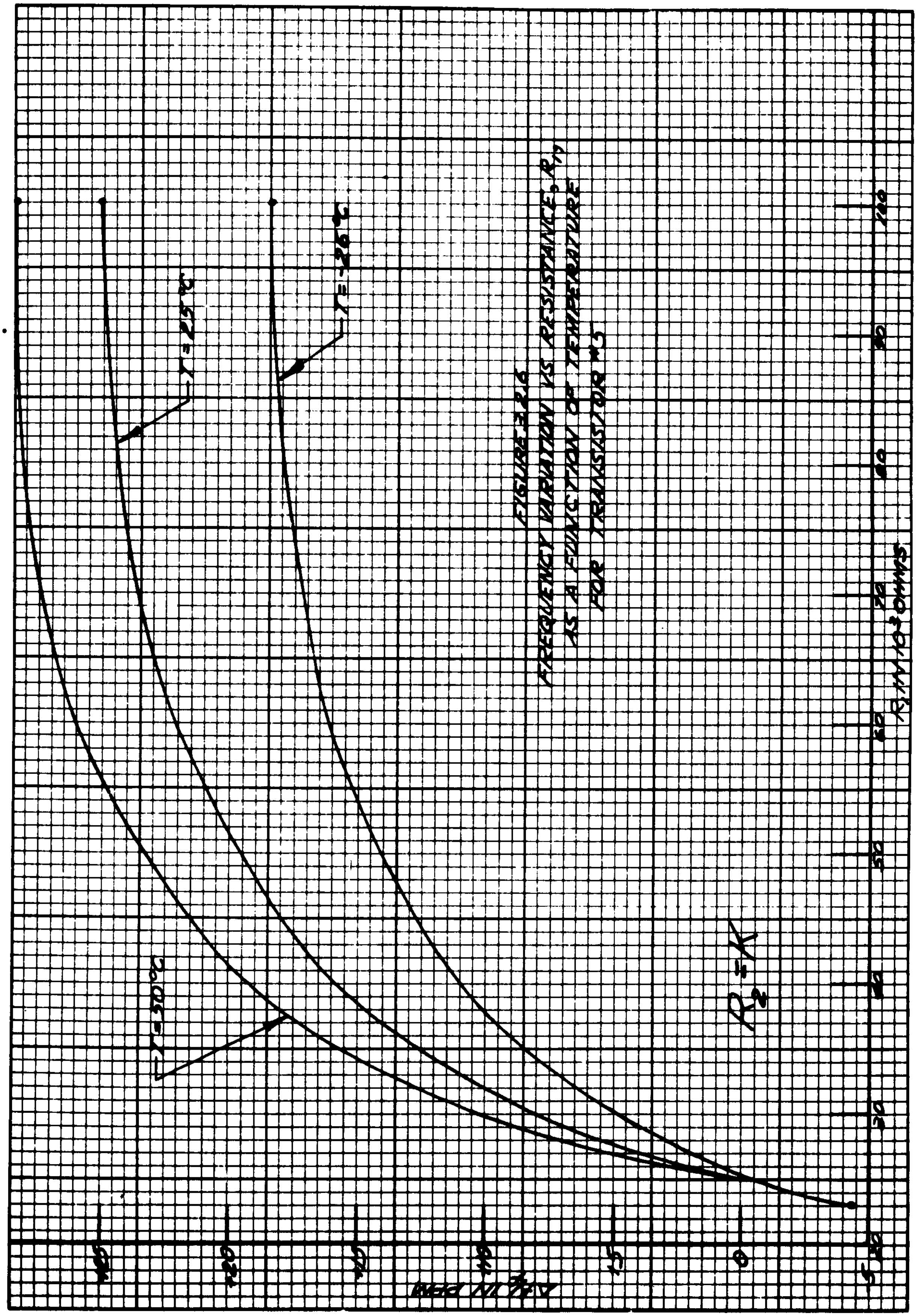


FIGURE 3.2.6
FREQUENCY VARIATION VS RESISTANCE, R_{19}
AS A FUNCTION OF TEMPERATURE
FOR TRANSISTOR #5

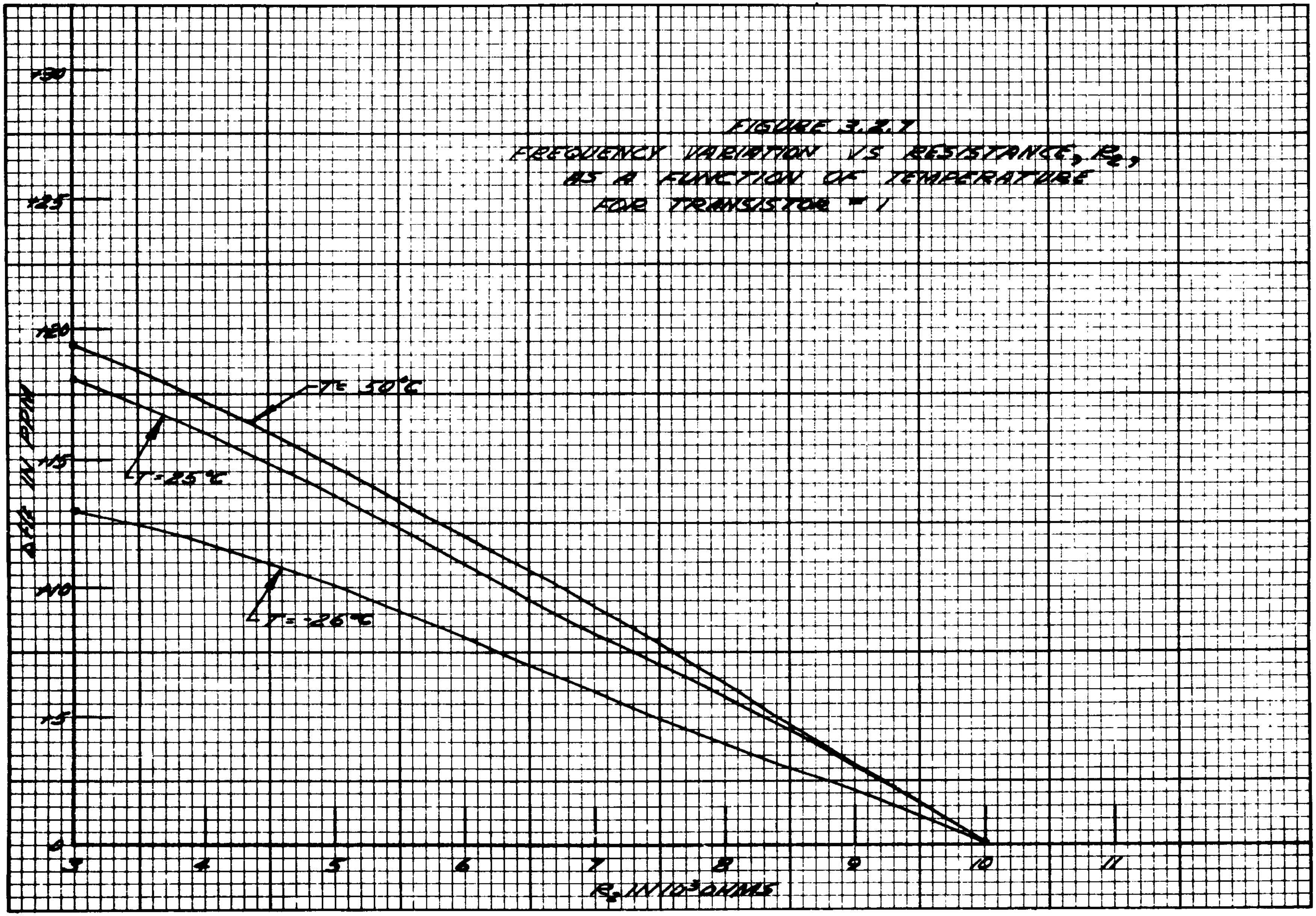


FIGURE 3.2.7
FREQUENCY VARIATION VS RESISTANCE, R_2,
AS A FUNCTION OF TEMPERATURE
FOR TRANSISTOR #1
T = 50°C
T = 25°C
T = -26°C
+30
+25
+20
+15
+10
+5
0
3
4
5
6
7
8
9
10
11
$\Delta f/f$ IN PPM
R_2 IN 10^3 OHMS

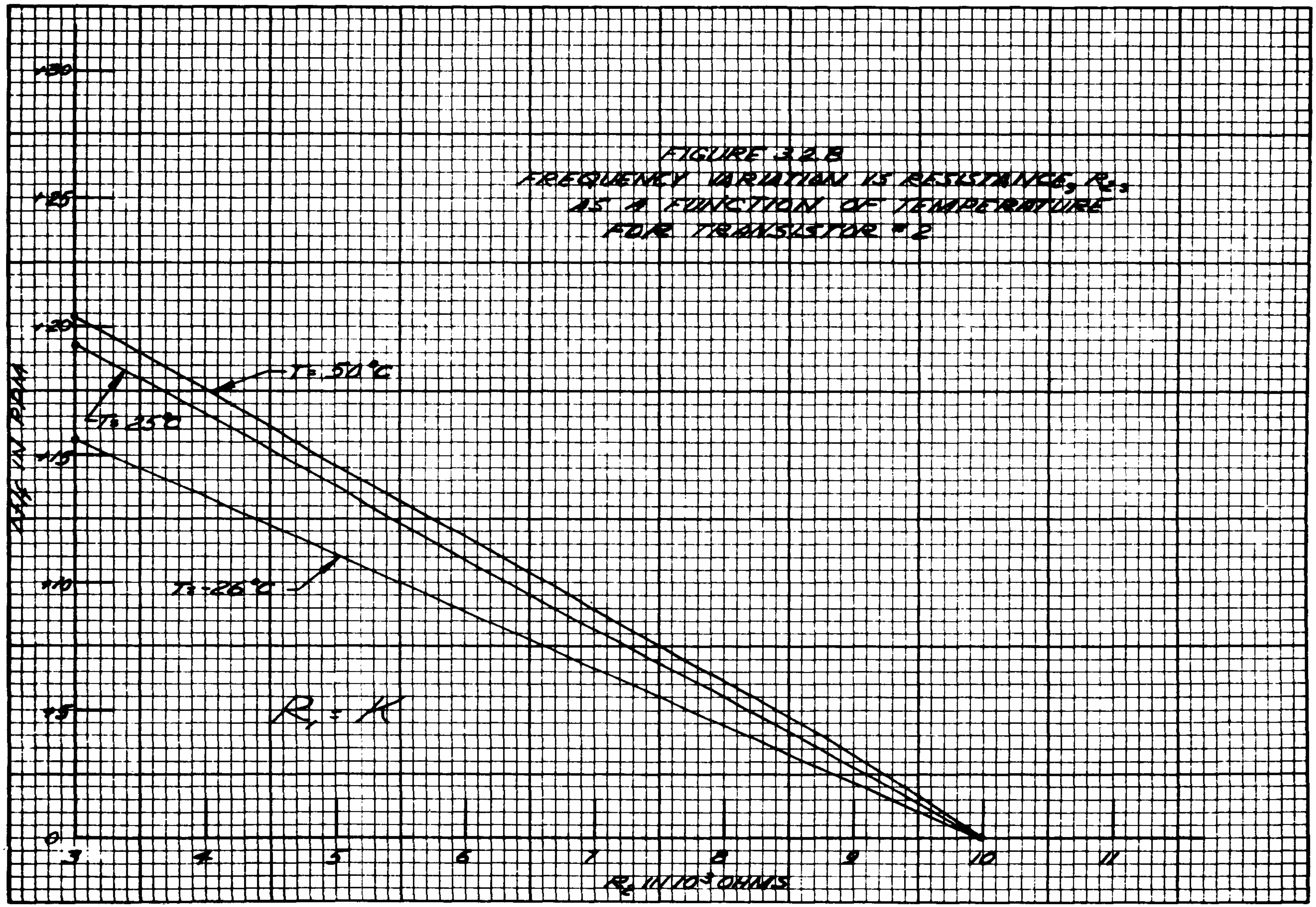


FIGURE 3.2.B
FREQUENCY VARIATION VS RESISTANCE, R_{e3}
AS A FUNCTION OF TEMPERATURE
FOR TRANSISTOR #2
T= 50°C
T= 25°C
T= -26°C
$R_1 = K$
+30
+25
+20
+15
+10
+5
0
3
4
5
6
7
8
9
10
11
R_e IN 10^3 OHMS
Δf IN PPM

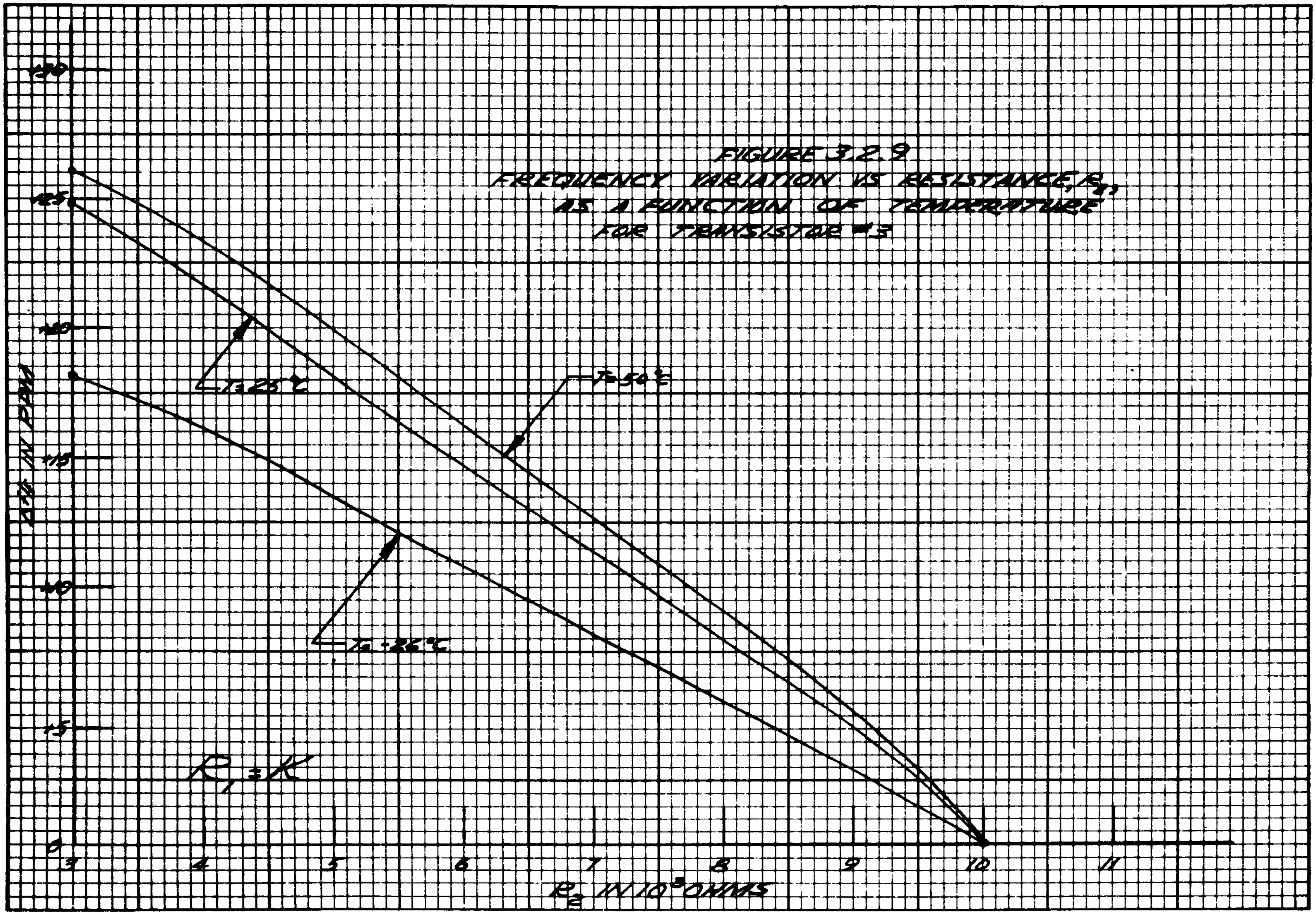


FIGURE 3.2.9
FREQUENCY VARIATION VS RESISTANCE, R_2,
AS A FUNCTION OF TEMPERATURE
FOR TRANSISTOR #3

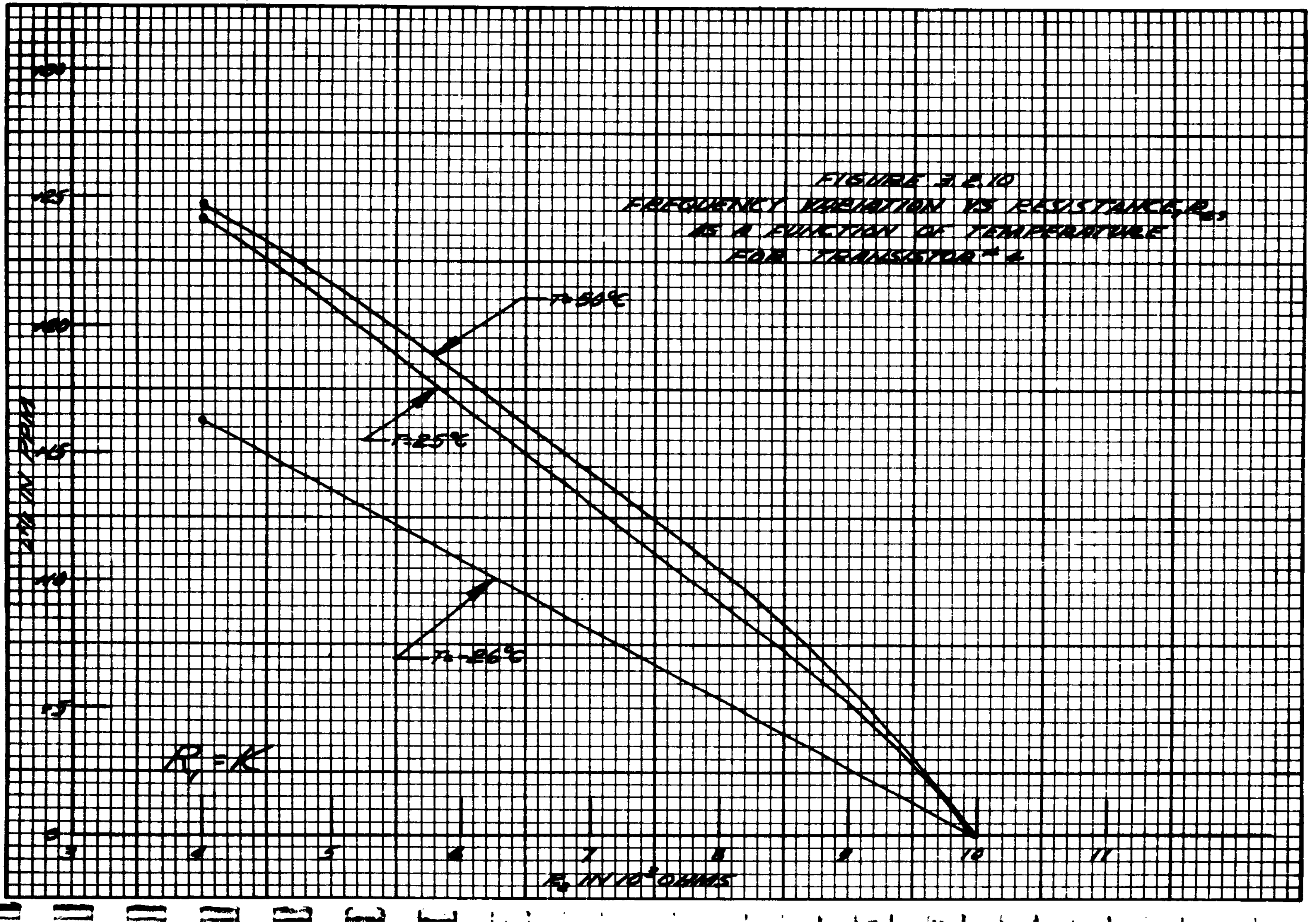


FIGURE 3.2.10
FREQUENCY VARIATION VS RESISTANCE,
AS A FUNCTION OF TEMPERATURE
FOR TRANSISTOR # 4

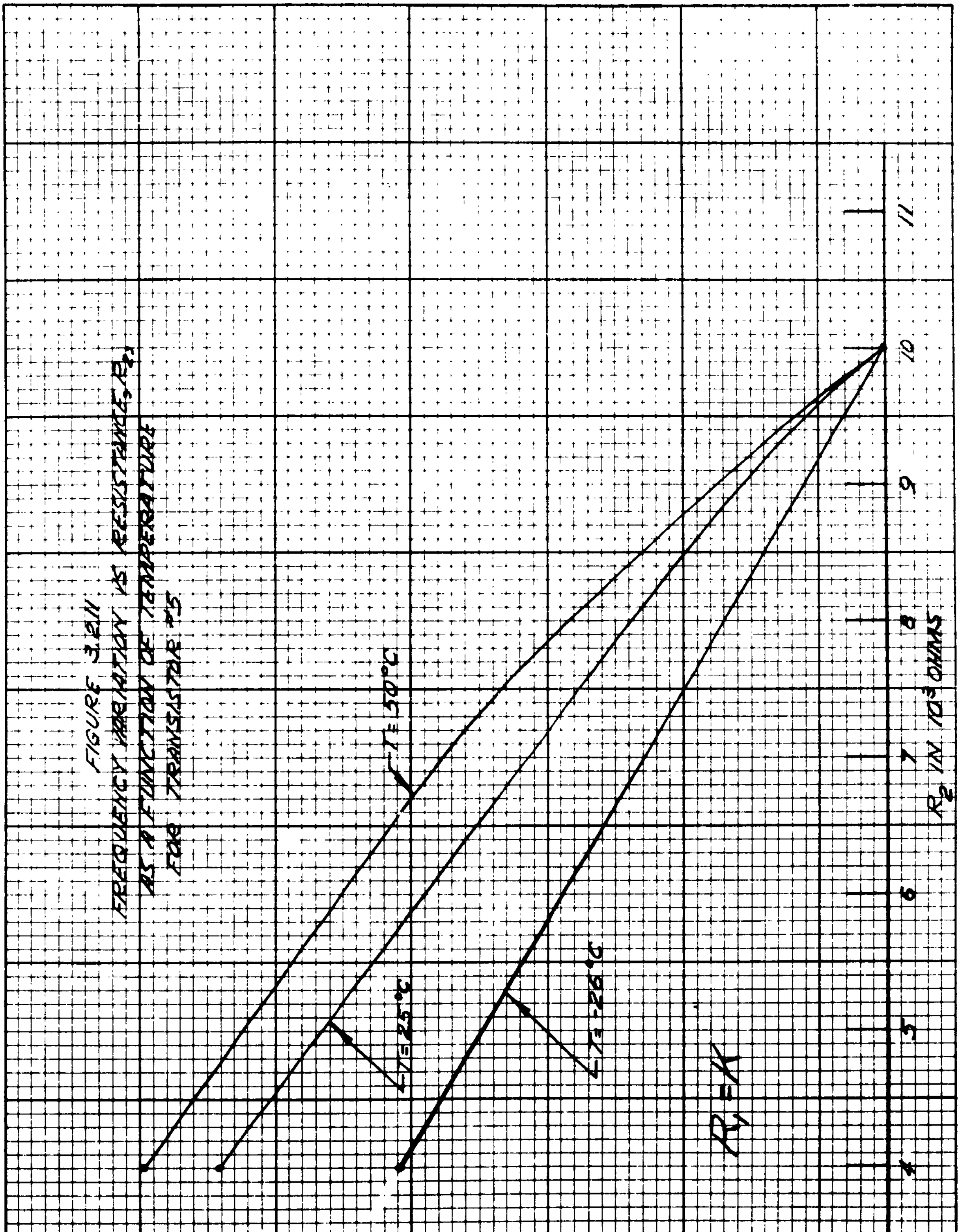


FIGURE 3.211
FREQUENCY VARIATION VS RESISTANCE, R_2,
AS A FUNCTION OF TEMPERATURE
FOR TRANSISTOR #5

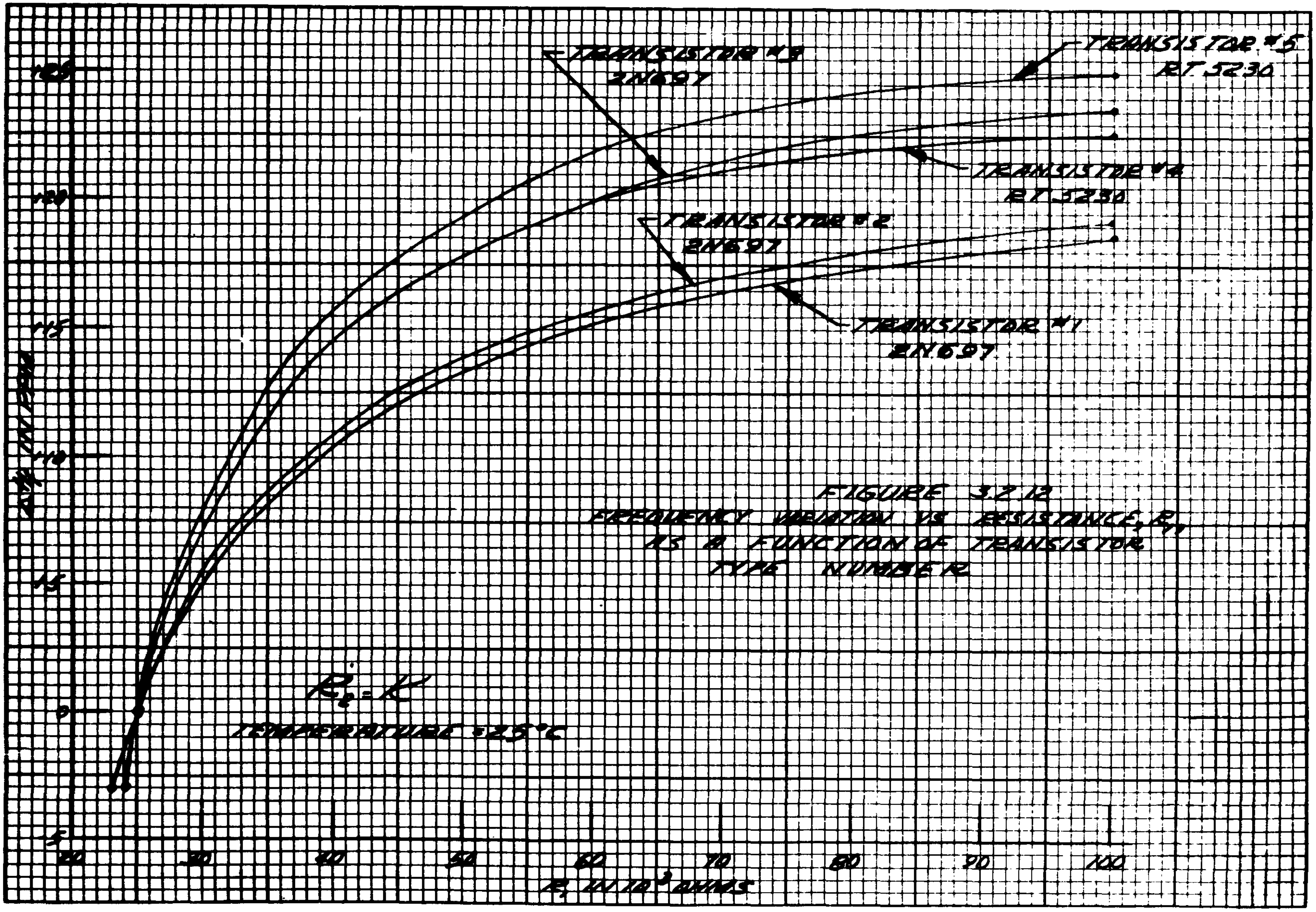


FIGURE 3.7.12
FREQUENCY VARIATION VS RESISTANCE, R_1
AS A FUNCTION OF TRANSISTOR
TYPE NUMBER

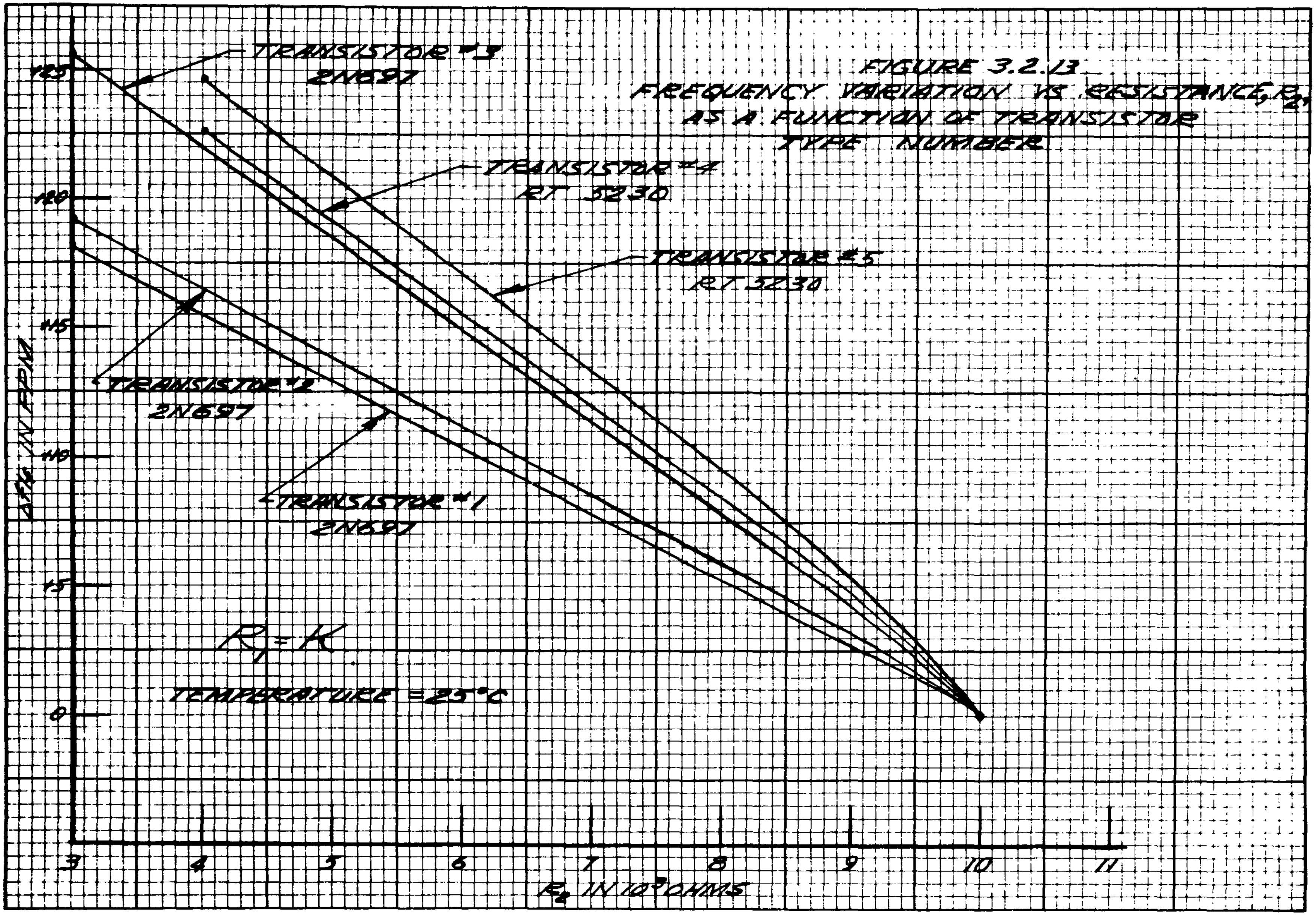


FIGURE 3.2.13
FREQUENCY VARIATION VS RESISTANCE, R_2, AS A FUNCTION OF TRANSISTOR TYPE NUMBER

incremental change in frequency for a given change in resistance. The temperature effects on the pullability of the various transistors is also only a matter of a difference in slope of the curves. In the previous Quarterly Report, it was shown that the beta of the transistor has an effect on the pullability of the transistor.

Table #2 indicates the effect of changing the oscillator bias voltage on the frequency of oscillation. The Δf/f versus voltage characteristics are recorded as a function of temperature with a constant bias.

Table #2

Transistor No.	Frequency Deviation (Δf/f) per Volt (Bias Voltage)		
	T = -26°C R_1 = 100K R_2 = 10K	T = 25°C R_1 = 25K R_2 = 10K	T = 50°C R_1 = 25K R_2 = 4K
1	+0.51	+0.25	+0.49
2	+0.51	+0.25	+0.48
3	+0.60	+0.02	+0.42
4	+0.40	-0.02	+0.31
5	+0.44	-0.11	+0.40

The transistor method has some advantages over the other methods of compensation. One is the simplicity of the circuit. A minimum number of components are used in the compensated oscillator. Another is the relative simplicity of the compensating thermistor-resistor networks, R_1 and R_2. There are limits on the magnitude of R_1 and R_2 placed by the transistor because there is a minimum gain that can be tolerated and operation must remain within those limits. The curve of R_1 versus temperature and R_2 versus temperature is easily approximated by a simple combination circuit with only minor variations from one transistor to the next if transistors were selected by checking the

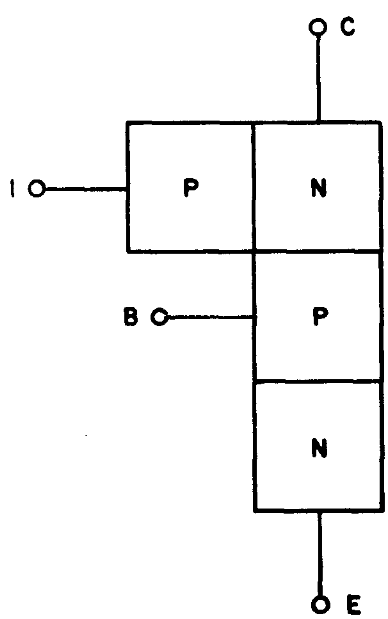
C_{cb} versus V_{cb} characteristics of each transistor.

There are also a number of disadvantages to the transistor method. The main one is that to obtain very close compensation, for example 1 PPM or better, more than one temperature run will be necessary in most cases. Also the value of thermistors may need to be changed for each transistor which precludes the use of a fixed standard compensation network. Another major problem that is encountered when using the transistor method for compensation is the voltage coefficient that is exhibited. A voltage variation of less than 1 volt is required to maintain a change less than 0.5 PPM. Even if the oscillator is temperature compensated, the best stability that could be obtained will be dictated by the voltage coefficient and voltage regulation of the oscillator.

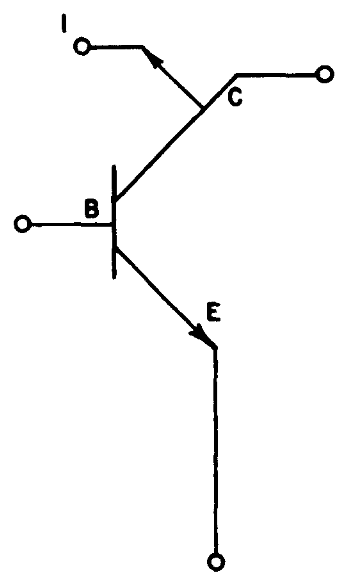
Using the isolation stage method of compensation in conjunction with the transistor method will increase the temperature stability, but the voltage effect will remain approximately the same. The transistor method appears to be a feasible method of compensation where stabilities with temperature of 1 PPM or larger are desired, but does not seem to be practical at this time for stabilities better than 1 PPM over the temperature range of -40°C to +70°C.

3.3 Binistor Compensation Method

The binistor method of compensation depends on the capacitance change of a semiconductor junction, as do the other methods of compensation. The primary difference between the binistor method and the other methods of compensation is that part of the junction to be used as a voltage variable capacitor is internal to the transistor and part is external. Figure 3.3.1(a) and 3.3.1(b) illustrate the manner in which a binistor is physically constructed and the electronic symbol for the binistor. The binistor is a PNPN device with leads attached to all four distinct areas. The binistor can be considered as a NPN transistor with a P-type semiconductor, call the injector, attached to the collector. The injector-collector junction is the junction to be used for compensation.



(a)
BINISTOR



(b)
BINISTOR ELECTRONIC SYMBOL

BINISTOR CONFIGURATION
Figure 3.3.1

The oscillator configuration can be the same as shown for the other type of compensation with the crystal connected to the collector through the injector terminal. By applying the proper biasing potential across the injector-collector junction, the capacitance of the junction will vary in such a manner that the oscillator will be compensated over temperature.

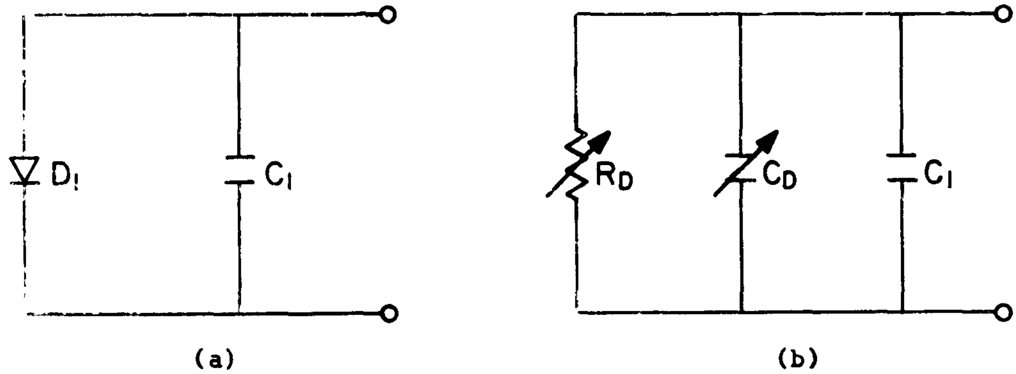
One problem associated with using the injector to collector junction as a voltage variable capacitance is that it cannot be DC isolated from the active network. The DC bias supply that provides V_{ic} has a path through the transistor as well as through the injector to collector junction.

Another problem is that binistors with large values of C_{ic} are not readily available. A test sample of five binistors, 3N57, were obtained and tested. All five had such low junction capacitances that they were not adequate for compensation purposes.

Further work on the binistor method of compensation is being postponed until it can be determined if binistors with larger values of C_{ic} are available.

3.4 Capacitor-Diode Compensation Method

During the last quarter the capacitor-diode method has been investigated more thoroughly. The analysis presented in the First Quarterly Report is not adequate to explain the entire phenomena of the capacitance change of the forward-biased diode in parallel with the fixed capacitor. In the previous analysis of the circuit in Figure 3.4.1(a), the effect of the diode capacitance was not considered. Figure 3.4.1(b) is a more accurate electrical equivalent circuit.

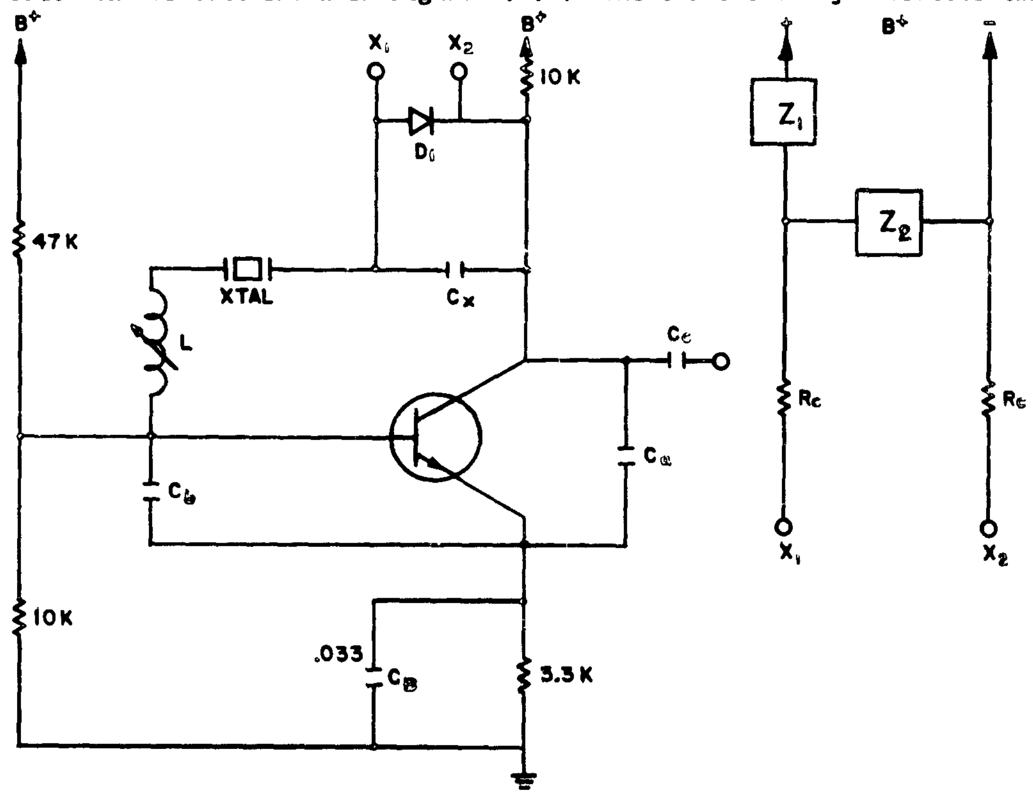


DIODE COMPENSATION NETWORKS
(a) WITHOUT AND (b) WITH DIODE CAPACITANCE SHOWN
Figure 3.4.1

Figure 3.4.1(b) shows C_1 as the external capacitor, C_D as the effective capacitance of the diode and R_D as the effective parallel a-c resistance of the diode. Both R_D and C_D will vary as the bias voltage is increased in the positive direction. R_D will decrease towards zero, C_D will increase towards infinity, and the sum $C_D + C_1$ will also increase towards infinity.

The bridge method of generating a control voltage discussed in the section on varicap compensation is also applicable to the capacitor-diode method. The fact that the bridge circuit allows operation through the zero bias point makes the capacitor-diode method more flexible. The analysis of the operation of the bridge in the forward direction proceeds along the same lines as the analysis for the varicap bridge circuit. Equations 24 and 25 in Section 3.1 for i_D and V_D are applicable when the diode is biased in the forward direction, but the assumption that Z_T = infinity made in Equations 26 and 27 cannot be made for the forward-biased diode. Z_T will vary from a very large value to a value approaching $2R_c$ and R_D will go from a very large value towards zero. The voltage across the diode biased in the forward direction can vary from zero to approximately one volt depending upon R_c and the diode.

A method of obtaining an almost zero voltage coefficient has been found. Consider the circuit shown in Figure 3.4.2. There are two major effects that



CAPACITOR-DIODE COMPENSATION CIRCUIT
Figure 3.4.2

change the frequency of the oscillator as the supply voltage is varied. One is the change in bias point of the compensating diode. As B+ is increased, the voltage across the diode increases, the capacitance exhibited by the diode increases and the frequency of oscillation decreases. Also, as B+ is increased the change in collector to base voltage is given by Equation 1 below, (Section 4.3, Equation 19 from the First Quarterly Report).

$$1) \quad \frac{dV_{cb}}{dE} \doteq \frac{R_1R_e - R_cR_2}{R_1R_e + R_2R_e + R_1R_2}$$

This equation indicates that the collector to base voltage can be increased or decreased with an increase in B+ or E depending on the values of R_1, R_2, R_e and R_c. The change in V_{cb} with a variation in supply voltage can be made zero if the following is true.

$$2) \quad R_1R_e = R_cR_2$$

If the V_{cb} is made to increase with an increase in B+, then the oscillator to base capacitance will decrease, increasing the frequency of the oscillator. The total change in frequency due to a change in B+ can be made very close to zero over a limited voltage range if the change in frequency due to the change in capacitance of the collector to base junction is adjusted to be equal to the change caused by the compensation network.

The curves in Figure 3.4.3 are the frequency versus supply voltage characteristics of an oscillator whose bias resistors have been adjusted to yield an almost zero voltage coefficient over a limited voltage range. The effect of temperature is shown in Figure 3.4.3. Over the temperature range of -40°C to +70°C a zero voltage coefficient is maintained for a supply voltage

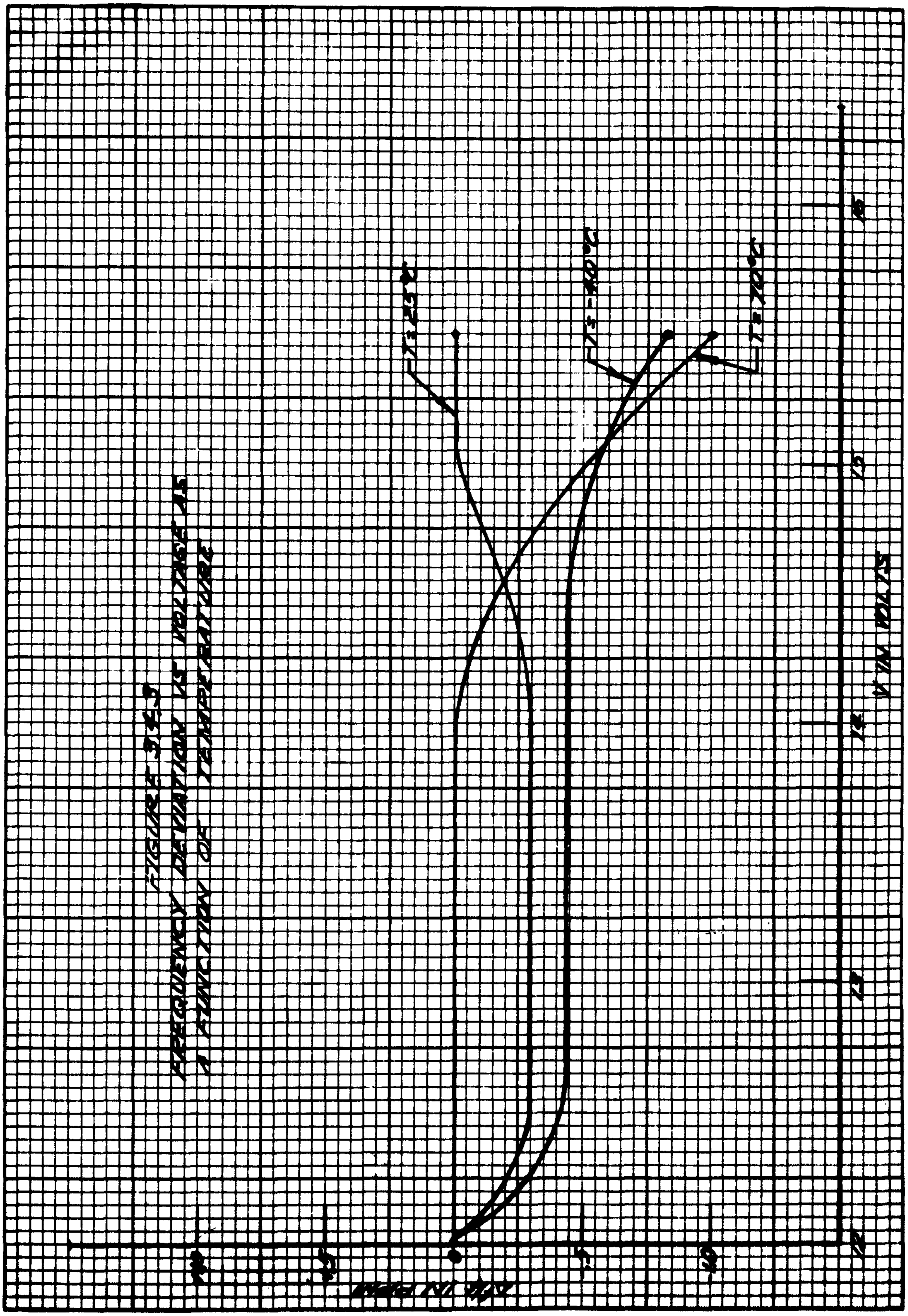


FIGURE 3.4.3
FREQUENCY DEVIATION VS VOLTAGE AS A FUNCTION OF TEMPERATURE

of from about 12.5 volts to 14 volts. Figure 3.4.4 shows the effect of varying the compensation network on the frequency versus supply voltage characteristics.

By establishing the proper bias point, a voltage coefficient of close to zero may be established. Consequently, this will reduce the amount of voltage regulation that is required for a compensated oscillator circuit. This method of obtaining a zero voltage coefficient may be used with the varicap method, but may not be used for the transistor method of compensation.

The compensation of an oscillator with specific circuits, components, crystals and compensation networks means that each oscillator has to be compensated individually. One way of decreasing the amount of time for compensation of a number of oscillators would be to obtain components with identical characteristics. If very close tolerances were placed on each component to be used in a compensated oscillator, interchanging components should have very little effect on the frequency items.

Obtaining components that have identical characteristics from unit to unit is difficult. It is nearly impossible to make a large number of crystals with identical frequency-temperature characteristics and C_o/C_1 ratios. The reverse and forward biased characteristics of diodes will vary slightly from one unit to another even if they are the same type. Thermistor beta and R_o will vary from unit to unit by certain amounts. All of these variations make it almost impossible to build a standard circuit for compensation with no provision for adjustment. No matter how close the tolerances are held on each component the variations will still be present and will effect the compensation afforded by a given design.

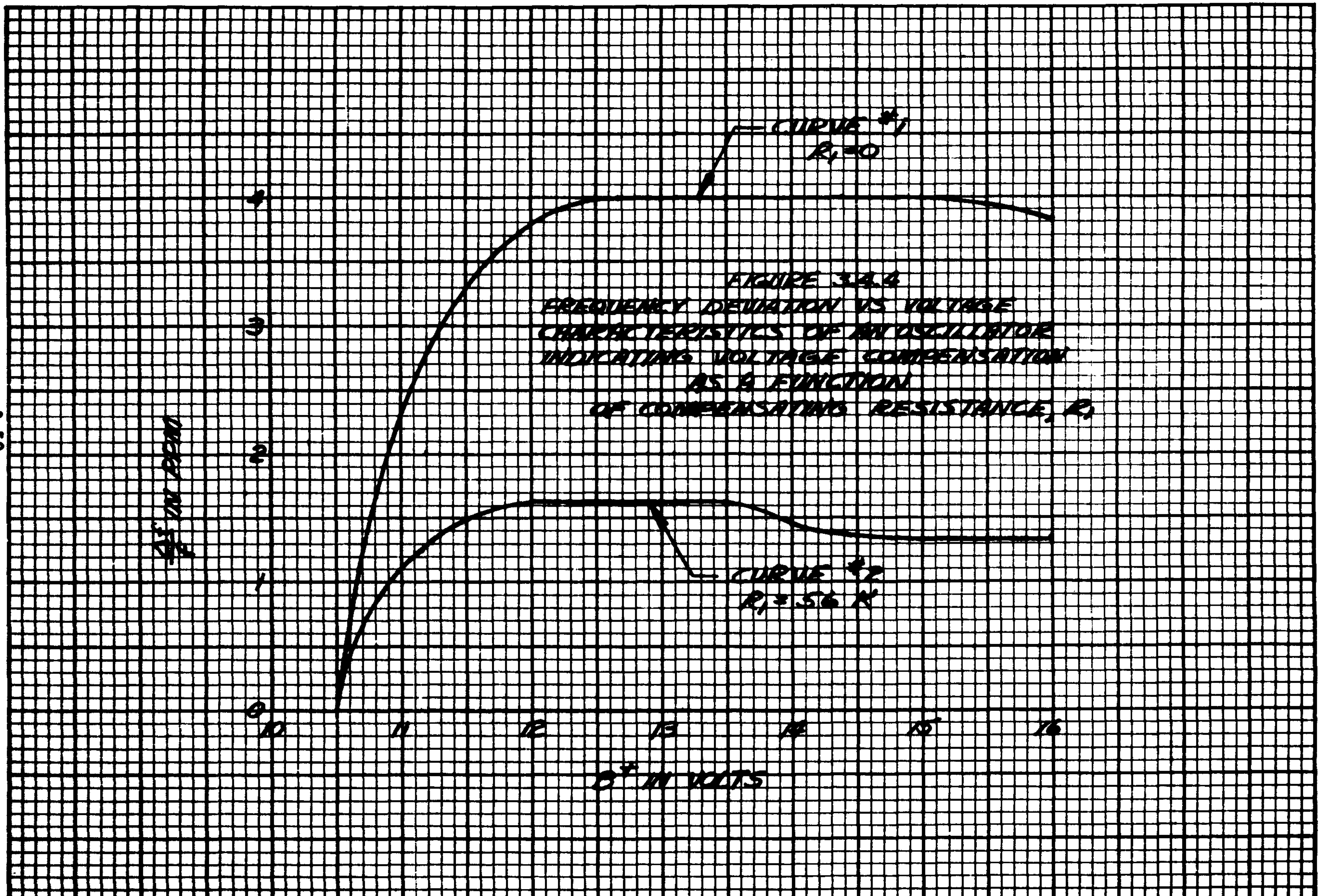


FIGURE 3.4.4
FREQUENCY DEVIATION VS VOLTAGE CHARACTERISTICS OF AN OSCILLATOR INDICATING VOLTAGE COMPENSATION AS A FUNCTION OF COMPENSATING RESISTANCE, R_1

Means other than giving extremely small tolerances on components must be devised before a standard circuit will be practical. In order to devise means of standardizing oscillator and compensation networks, a study has been initiated. The parameters that affect compensation and the parameters that can be varied to adjust for differences in components are being investigated.

The crystal is the major element in any compensated oscillator. The frequency-temperature curves of the crystal dictates the compensation that is needed. The C_o/C_1 ratio of the crystal determines the capacitance change with temperature required to compensate the frequency temperature characteristics of the crystal. Once a crystal has been obtained and is to compensated, there is little that can be done to change its characteristics. Therefore, adjustments for the difference between crystal characteristics must be made elsewhere in the oscillator. The capacitance versus voltage curve for a diode determines the voltage or resistance versus temperature characteristics that are required for compensation. Since the diode characteristics cannot be altered, the thermistor-resistor network is the only part of the oscillator that is left to provide adjustment. If a standard thermistor-resistor network is to be used, then either the supply voltage must be used for adjustment or existing or additional networks must be used to adjust for variations in component parameters.

When there is a wide variation in the crystal's parameters, it will be necessary to alter the thermistors in the thermistor-resistor network and possibly to change the diode. When the crystal's parameters do not vary widely, it may not be necessary to alter thermistors, but the resistor values may have to be changed. One of the possibilities of having a standardized compensation circuit is to provide variable resistors in the thermistor-resistor network.

The other possibility mentioned previously of having an additional network in the compensation circuit to correct for changes in component parameters is also feasible. The capacitor diode method has a built-in correction network. The decoupling resistors, R_c in Figure 3.4.2(b), directly affect the slope of the $\Delta f/f$ versus R curves for the compensation networks. By varying the value of R_c, the $\Delta f/f$ versus R characteristics of the compensation network can be altered over a wide range because this, in effect, changes the magnitude of the current through the diode and, consequently, the effect of the resistance. Also the capacitor across the diode affects the $\Delta f/f$ versus R characteristics of the diode. By using both of these means of adjusting the pullability of the compensation network and variable resistors in the compensation network. Adjustment for a wide range of component parameters should be obtainable.

One other possibility that exists for correcting for component variations is to use a TC capacitor. Using a TC capacitor across the crystal can effectively change the apparent angle of cut of the crystal. Thus by selecting values of TC capacitors, a group of crystals can be made to have almost identical temperature characteristics. Also if a component variation causes an error in compensation of a constant slope, a TC capacitor may provide a means of correcting the error in slope. The methods discussed correcting for errors due to component variations is not restricted to the capacitor diode method but are general in nature.

A number of tests were conducted on various phases of the capacitor diode compensation techniques. Figure 3.4.5 is a plot of the $\Delta f/f$ versus temperature characteristics of a temperature compensated three megacycle oscillator. The schematic for the oscillator circuit used to obtain the curves in Figure 3.4.5 is shown in Figure 3.4.6. Previously, R_1 and R_2 have

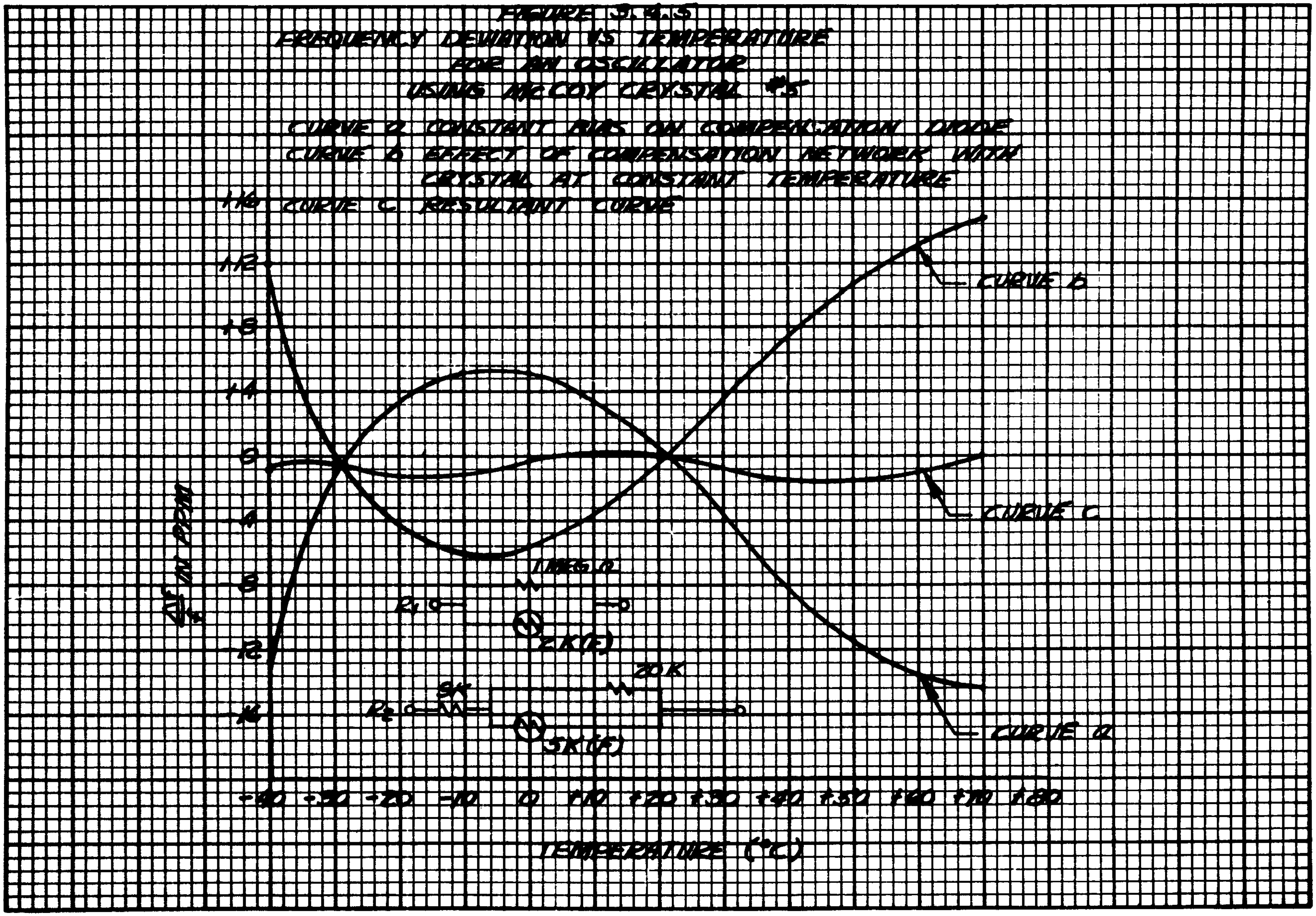
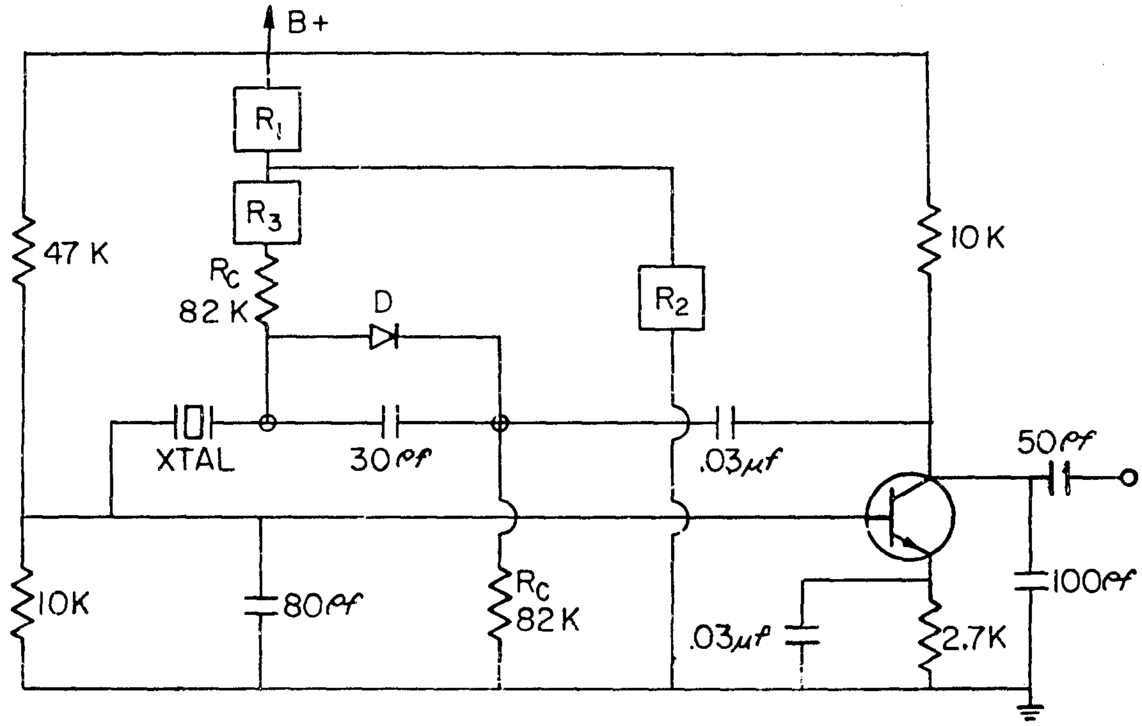


FIGURE 3.4.5
FREQUENCY DEVIATION VS TEMPERATURE
FOR AN OSCILLATOR
USING McCOY CRYSTAL #5

CURVE a CONSTANT BIAS ON COMPENSATION DIODE
CURVE b EFFECT OF COMPENSATION NETWORK WITH
CRYSTAL AT CONSTANT TEMPERATURE
CURVE C RESULTANT CURVE

been used for compensation purposes. In this instance, instead of using R_1 for compensation at the low temperature range, another compensation element,



SCHEMATIC FOR CAPACITOR-DIODE COMPENSATION METHOD
Figure 3.4.6

R_3, was used. R_3 is connected in series with the decoupling resistor, R_c. For some particular crystal frequency-temperature characteristics, it seems that the use of R_3 for compensation instead of R_1 provides a simpler approach to compensation. Figure 3.4.7 is a comparison of the $\Delta f/f$ versus R characteristics of R_1 and R_3. Figures 3.4.8 and 3.4.9 are plots of the $\Delta f/f$ versus R_2 and R_3 characteristics of the oscillator shown in Figure 3.4.6. These curves were the ones used for obtaining the curves shown in Figure 3.4.5.

Curve (a), shown in Figure 3.4.5, is the frequency versus temperature characteristics of the uncompensated oscillator of Figure 3.4.6. Curve (b) is a plot of the frequency versus temperature characteristics of the oscillator using the compensation networks shown, but the crystal frequency-temperature

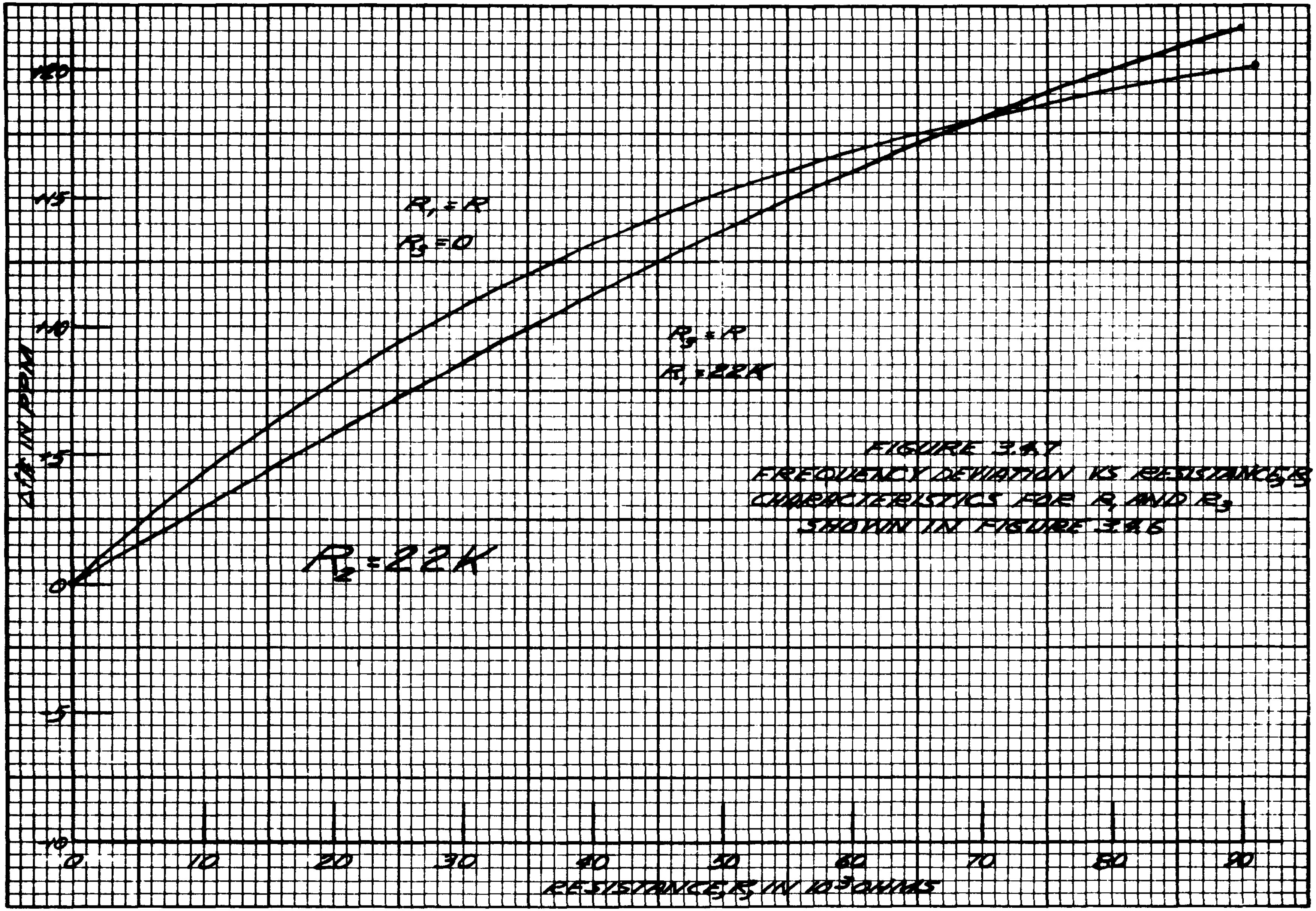


FIGURE 3.47
FREQUENCY DEVIATION VS RESISTANCE, R
CHARACTERISTICS FOR R_1 AND R_3
SHOWN IN FIGURE 3.46

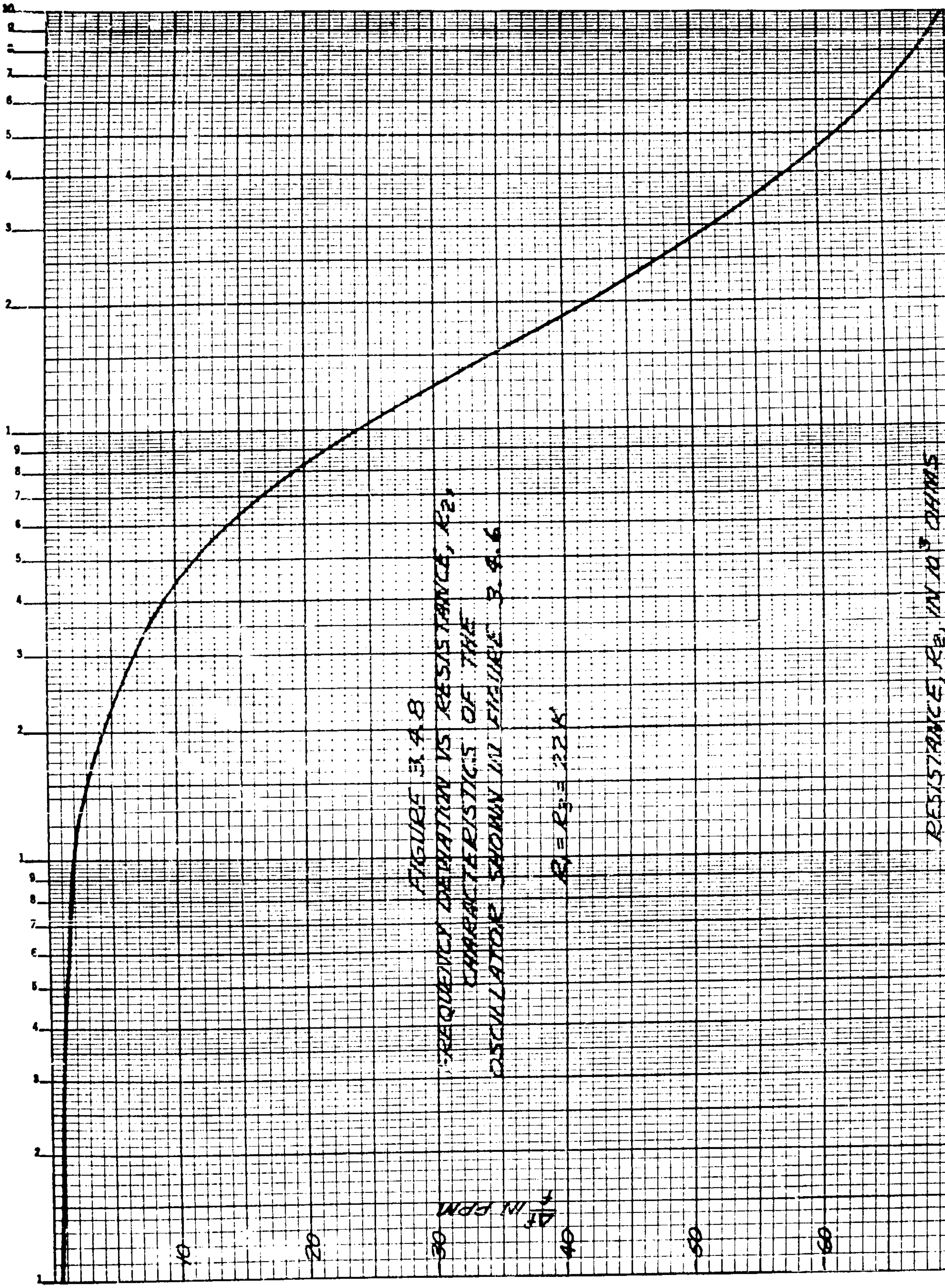


FIGURE 3.4.8
FREQUENCY DEVIATION VS RESISTANCE, R2, CHARACTERISTICS OF THE OSCILLATOR SHOWN IN FIGURE 3.4.6

$R_1 = R_3 = 22K$

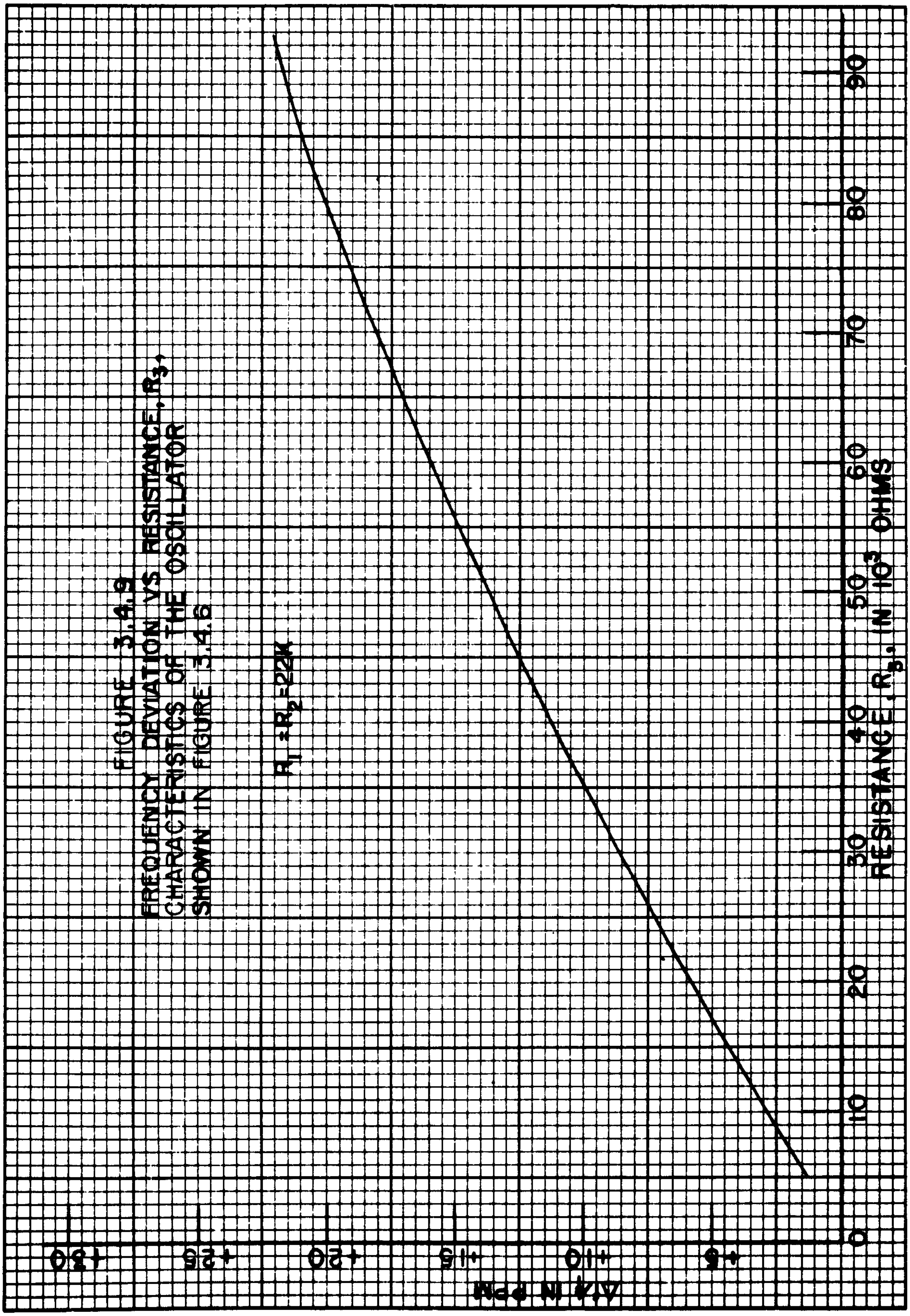


FIGURE 3.4.9
FREQUENCY DEVIATION VS RESISTANCE, R_3, CHARACTERISTICS OF THE OSCILLATOR SHOWN IN FIGURE 3.4.6

$R_1 = R_2 = 22K$

characteristics eliminated. Curve (c) is a plot of the resultant characteristics of the compensated oscillator.

As can be seen from the compensation networks shown in Figure 3.4.5, the networks are a simple combination of a total of two thermistors and three resistors. Figure 3.4.10 is a plot of the calculated R versus temperature characteristics of the two networks.

The results of tests that have been conducted indicate that the diode has a temperatue effect upon the compensation curves. Figure 3.4.11 is a frequency deviation versus temperature curve that resulted from a capacitor-diode compensation network with a constant bias. The results from the tests so far are not conclusive, but it appears that some diode types have less temperature effect than others.

The problem of compensating crystals with different frequency-temperature characteristics using the capacitor-diode compensation method is being investigated. Two crystal frequency versus temperature curves were taken from the reference chart of crystal characteristics shown in Figure 3.4.12, Curves #4 and #6, and the error curve in Figure 3.4.11 was added to these two curves. Figure 3.4.13 shows the resulting frequency-temperature characteristics.

The two curves shown in Figure 3.4.13 were assumed to be the curves of the oscillator in Figure 3.4.6. The characteristics were then compensated for by using the pullability curves of Figure 3.4.8 and 3.4.9. The results of the compensation procedure are shown in Figure 3.4.14. The networks required for compensation are also shown. The maximum deviation for both of the compensated oscillator curves is almost identical and this was achieved by changing only two resistors in the compensation network. The thermistors did not have to be changed. This indicates that a compensation network configuration and the thermistors could be specified for a certain

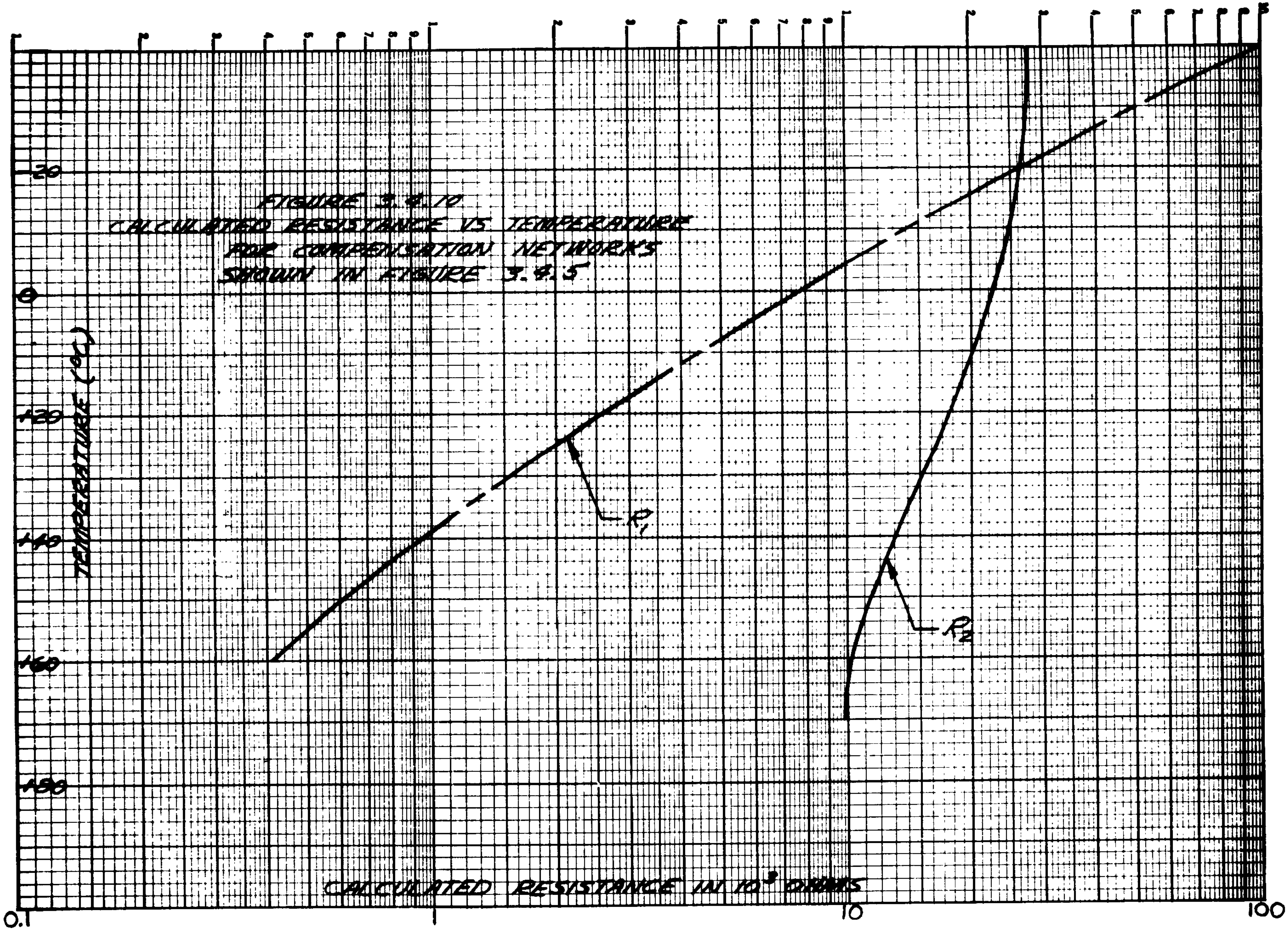


FIGURE 3.4.10
CALCULATED RESISTANCE VS TEMPERATURE
FOR COMPENSATION NETWORKS
SHOWN IN FIGURE 3.4.5

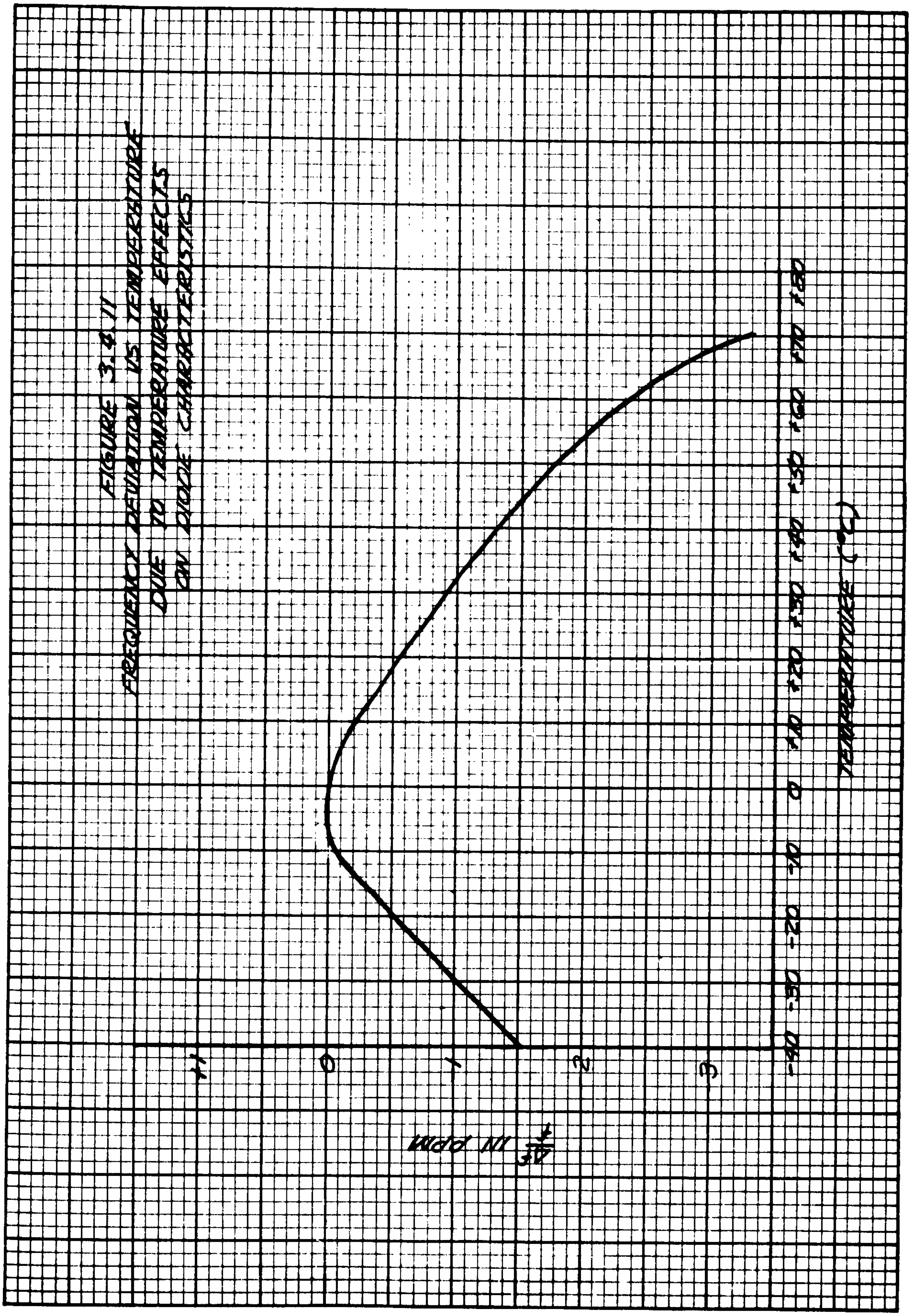


FIGURE 3.4.11
FREQUENCY DEVIATION VS TEMPERATURE
DUE TO TEMPERATURE EFFECTS
ON DIODE CHARACTERISTICS

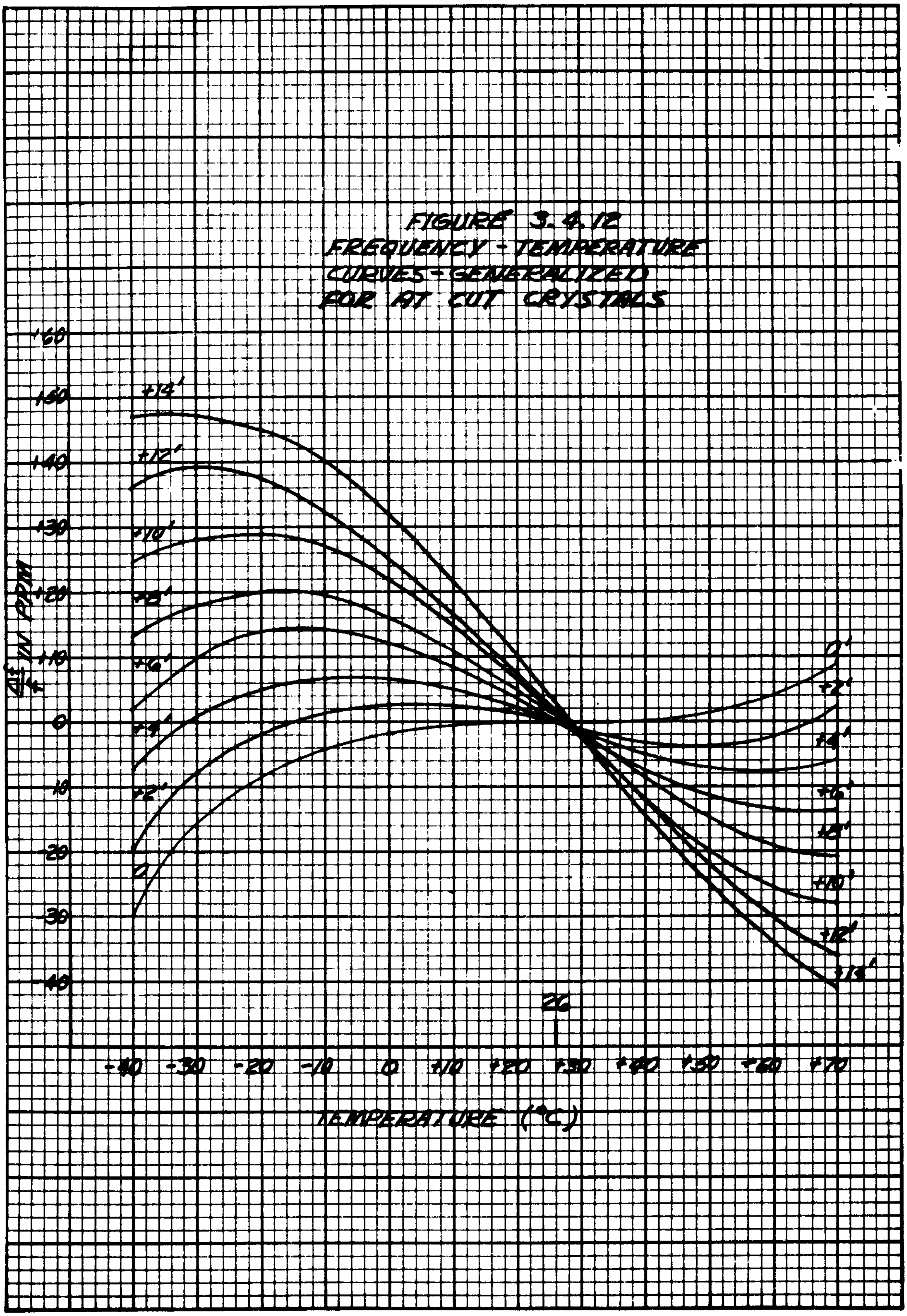
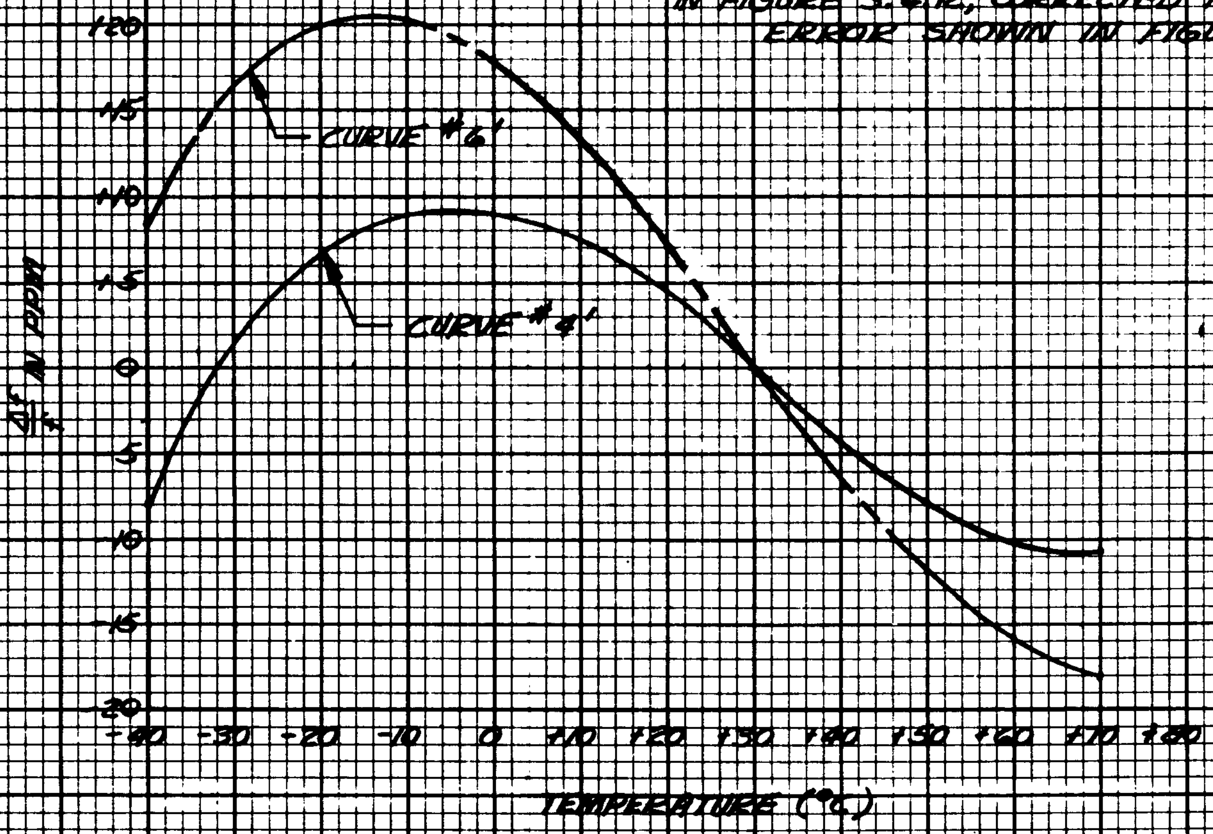


FIGURE 3.4.12
FREQUENCY - TEMPERATURE
CURVES - GENERALIZED
FOR AT CUT CRYSTALS
+60
+50
+40
+30
+20
+10
0
-10
-20
-30
-40
$\frac{\Delta f}{f}$ IN PPM
+14'
+12'
+10'
+8'
+6'
+4'
+2'
0'
26
-40
-30
-20
-10
0
+10
+20
+30
+40
+50
+60
+70
TEMPERATURE (°C)

FIGURE 3.4.13
FREQUENCY DEVIATION VS TEMPERATURE
CHARACTERISTICS OF CURVES #4' AND #6'
IN FIGURE 3.4.12, CORRECTED FOR THE DIODE
ERROR SHOWN IN FIGURE 3.4.11



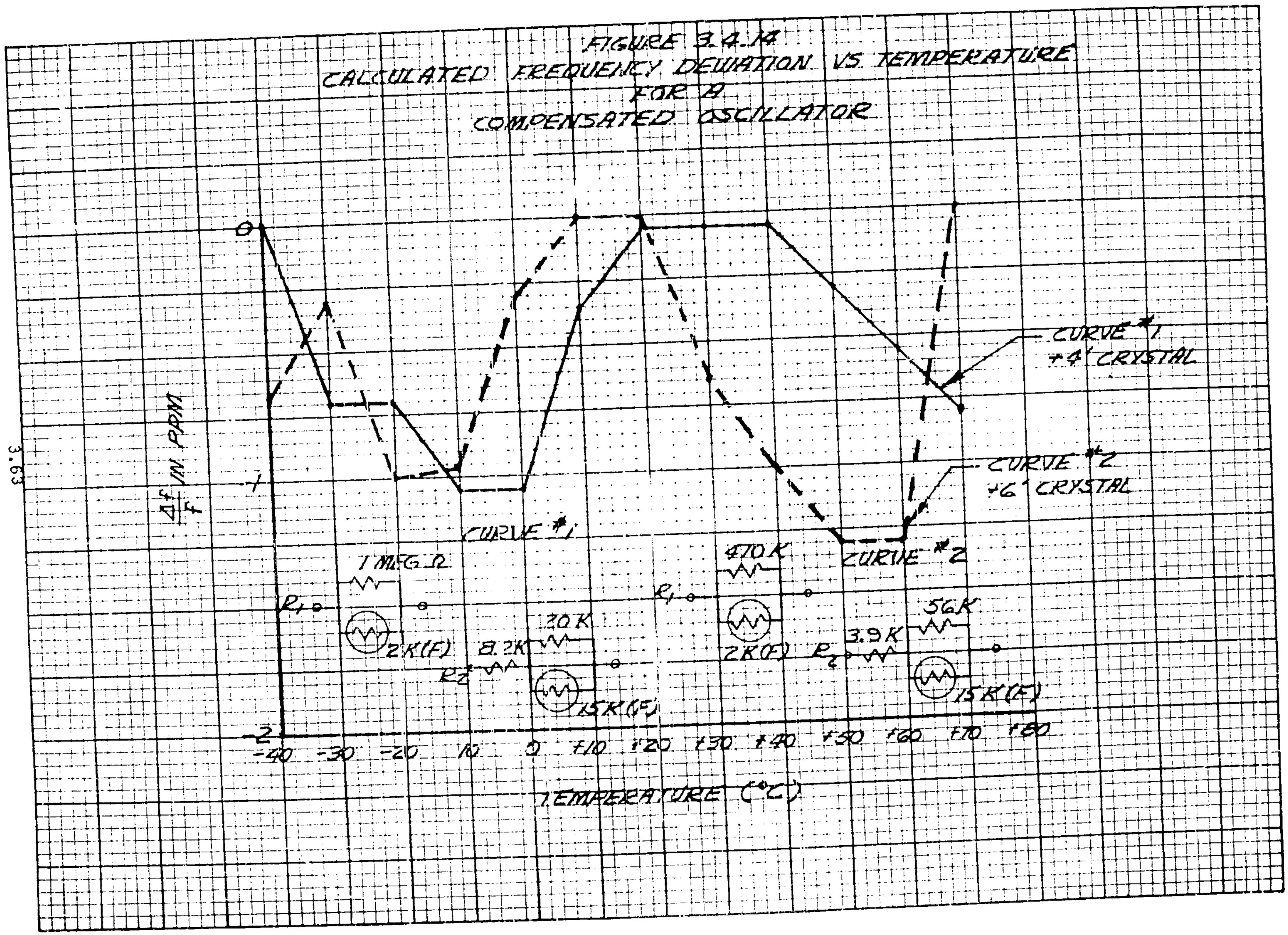


FIGURE 3.4.14
CALCULATED FREQUENCY DEVIATION VS TEMPERATURE
FOR A
COMPENSATED OSCILLATOR

spread of crystal characteristics and that changing fixed resistor values could compensate for the corresponding spread in crystal characteristics.

A number of types of diodes have been tested for uniformity in compensation characteristics. Figure 3.4.15 is a plot of $\Delta f/f$ versus R for a sample lot of 1N459 diodes. This diode type exhibited the best results from on ediode to another. A lot of ten 1N459 diodes was tested. The five shown in Figure 3.4.15 are typical and the other five diode's characteristics fell within the two extremes shown.

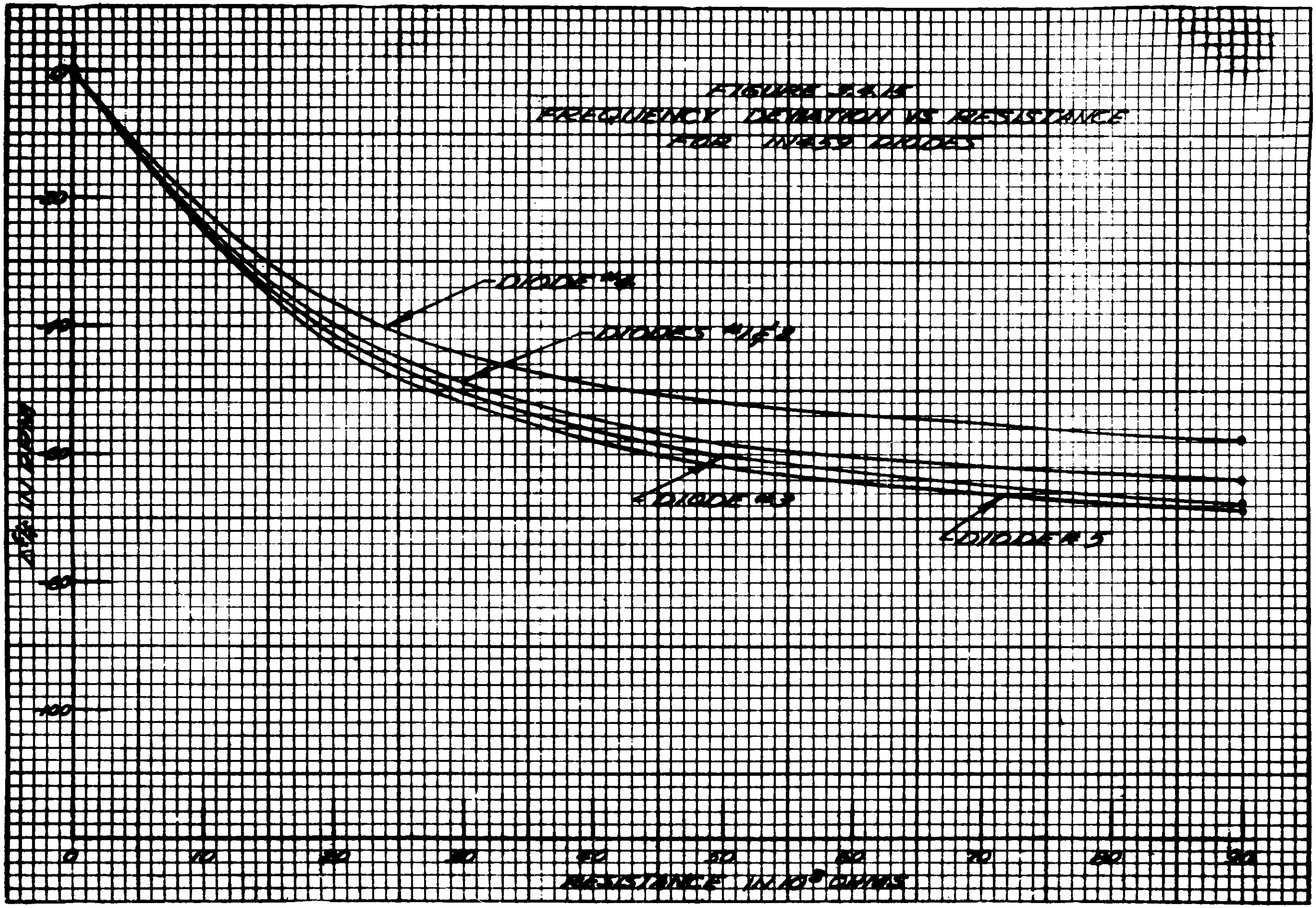
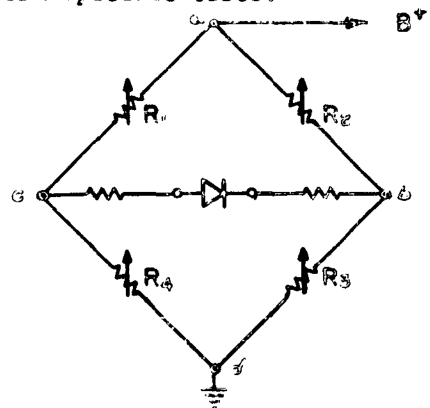


FIGURE 3.4.15
FREQUENCY DEVIATION VS RESISTANCE
FOR 1N459 DIODES
DIODE #4
DIODES #1 & 2
DIODE #3
DIODE #5
RESISTANCE IN 10³ OHMS
0
10
20
30
40
50
60
70
80
90

3.5 Diode Voltage Control and Switching

The voltage and current control bridge circuit analysis was presented in a previous section. A test circuit was built to empirically determine the characteristics of the zener diode controlled bridge. Figure 3.5.1 is a schematic of this circuit. The zener diodes were placed across the appropriate resistors to perform specific tests.



BRIDGE CIRCUIT
FIGURE 3.5.1

One of the problems that was anticipated using zener diodes as voltage limiters is that if the resistance of the circuit or the resistance in series with the zener is too large, then the zener voltage may not take control fast enough because of the limited current through the zener diode. The other extreme, when the resistance of the circuit is too small, may also be a problem. If the resistance is too small, an excessive amount of power will be drawn from the power supply. The zener increases the current drain from the power supply when it is biased well over the zener knee on its zener characteristic curve because a small increase in voltage causes a very large amount of additional current to be drawn through the zener.

Another point that was anticipated to have an effect on the voltage control of the zener diode is when the diode is forward biased. The current through the diode may upset the relatively isolated properties of the two voltage dividers present in the bridge. The current voltage relationship of a diode is shown in Figure 3.5.2. Due to the non-symmetrical properties of the diode, the characteristics of the bridge will not be the same when the diode is forward biased as when the diode is reverse biased.

A number of bridge circuits were built using various component values and the characteristics of each were investigated. Some of the typical curves are presented in this report. Figure 3.5.1 is a schematic of the basic circuit used for the data presented in the graphs with the appropriate modifications in the circuit indicated on each graph. Figure 3.5.3 is a plot of the voltage from point (a) to point (b) in Figure 3.5.1 and the total current into the bridge circuit versus the bridge resistance R_4. Curve (a) indicates the voltage versus R_4 relationship of the bridge without a zener diode and curve (b) indicates the voltage versus R_4 relationship with a 1N751 diode from point (a) to point (b). The zener has a pronounced effect on the voltage-resistance characteristics of the bridge. Curves (c) and (d) indicate the bridge current with and without the zener diode present, indicating that the current increases quite rapidly with the zener in the circuit as the resistance R_4 is decreased due to the zener characteristics.

Figure 3.5.4 indicates the effect of the zener on the bridge circuit when R_2 and R_4 are varied. The slopes of the V_{ac} versus R curves for R_2 and R_4 are almost identical but opposite in sign. The effect of different zener diodes on the voltage versus resistance characteristics of the bridge circuit is shown in Figure 3.5.5. The sharpness of the change in slope of the V versus R curve increases as the zener voltage of the diode increase which is quite evident in Figure 3.5.5.

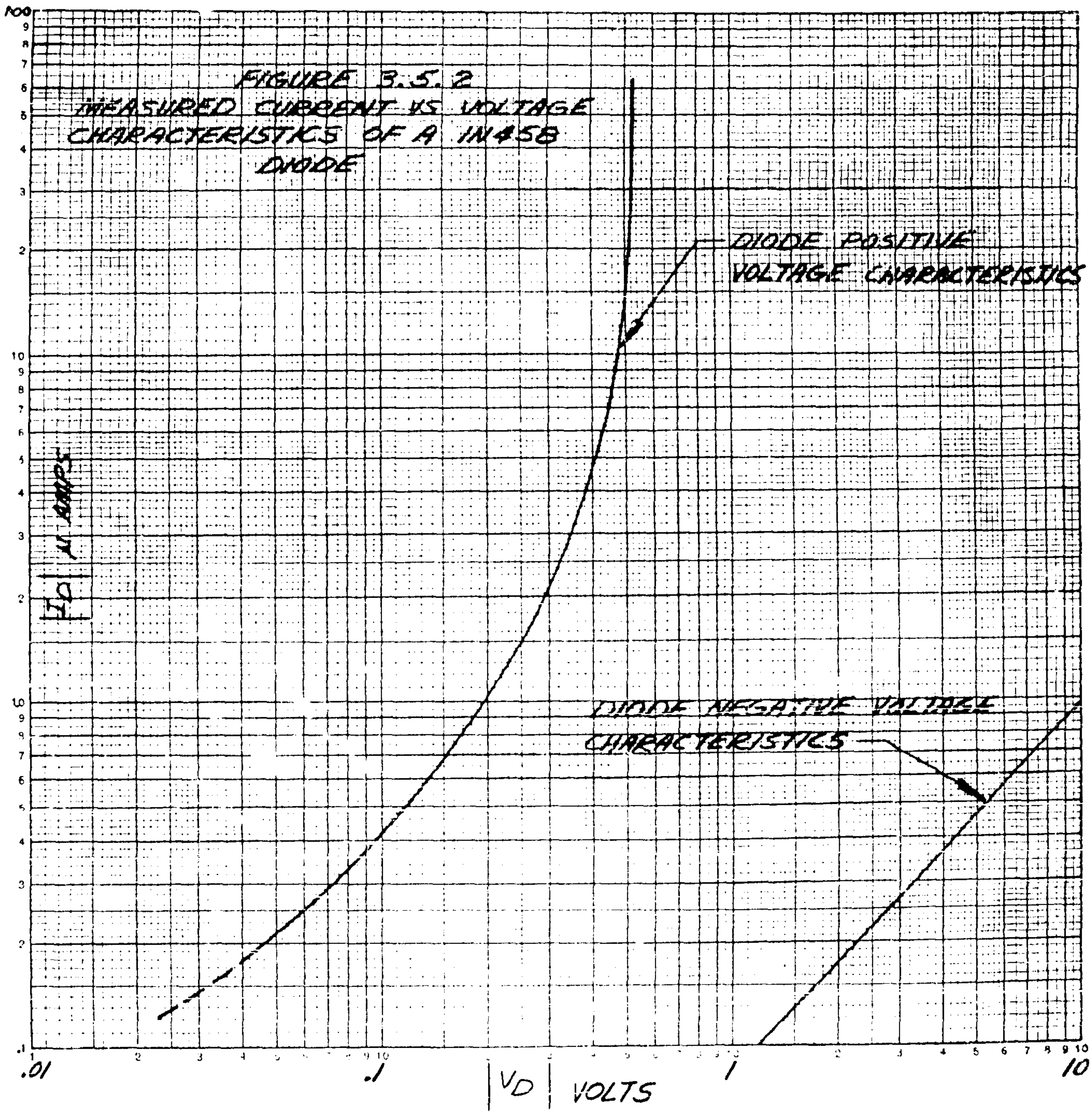


FIGURE 3.5.2
MEASURED CURRENT VS VOLTAGE
CHARACTERISTICS OF A 1N458
DIODE
DIODE POSITIVE
VOLTAGE CHARACTERISTICS
DIODE NEGATIVE VOLTAGE
CHARACTERISTICS
|I_D| µ AMPS
|V_D| VOLTS
.01
.1
1
10
100
10
1.0
.1

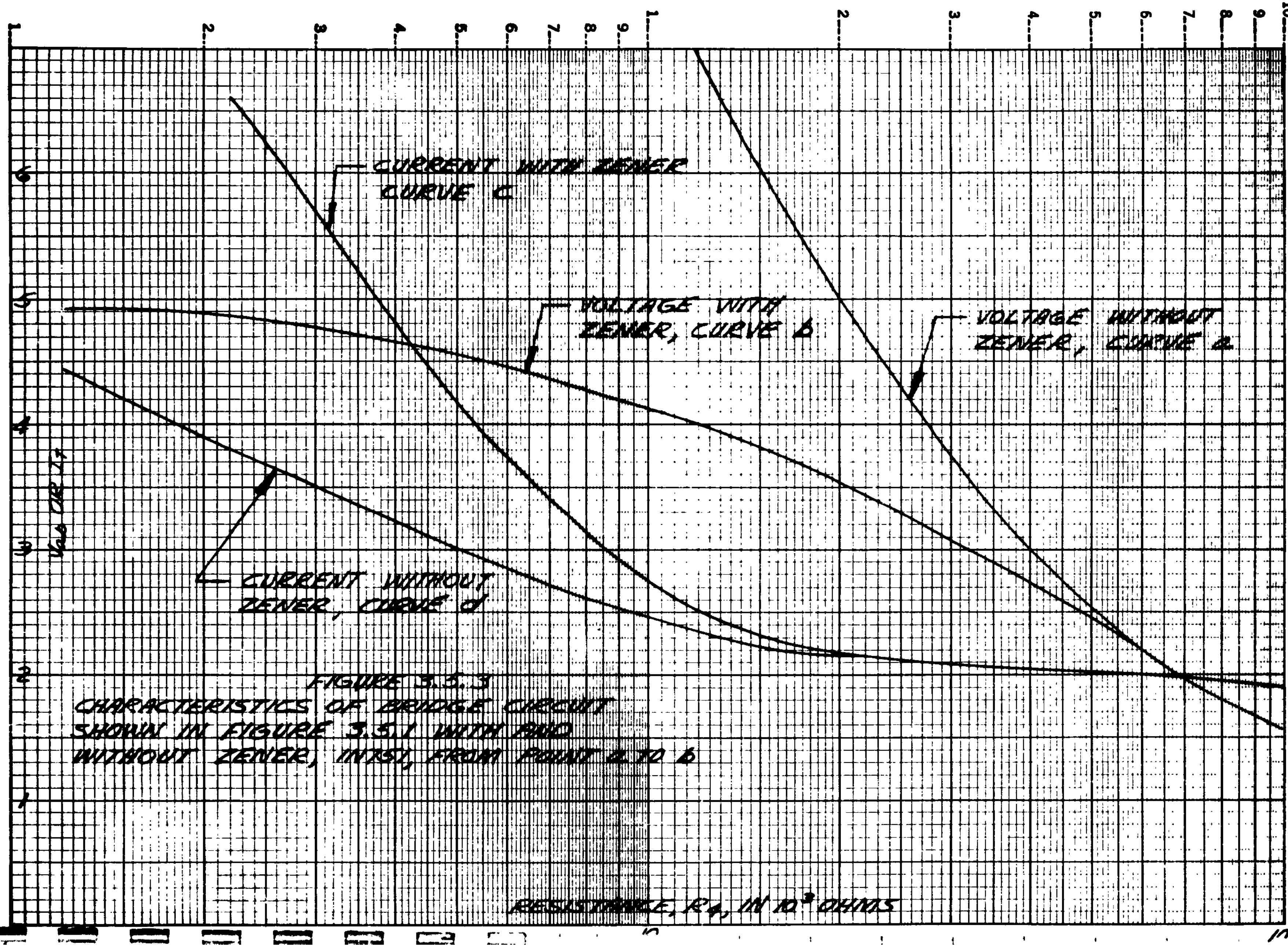


FIGURE 3.5.3
CHARACTERISTICS OF BRIDGE CIRCUIT
SHOWN IN FIGURE 3.5.1 WITH AND
WITHOUT ZENER, IN351, FROM POINT a TO b

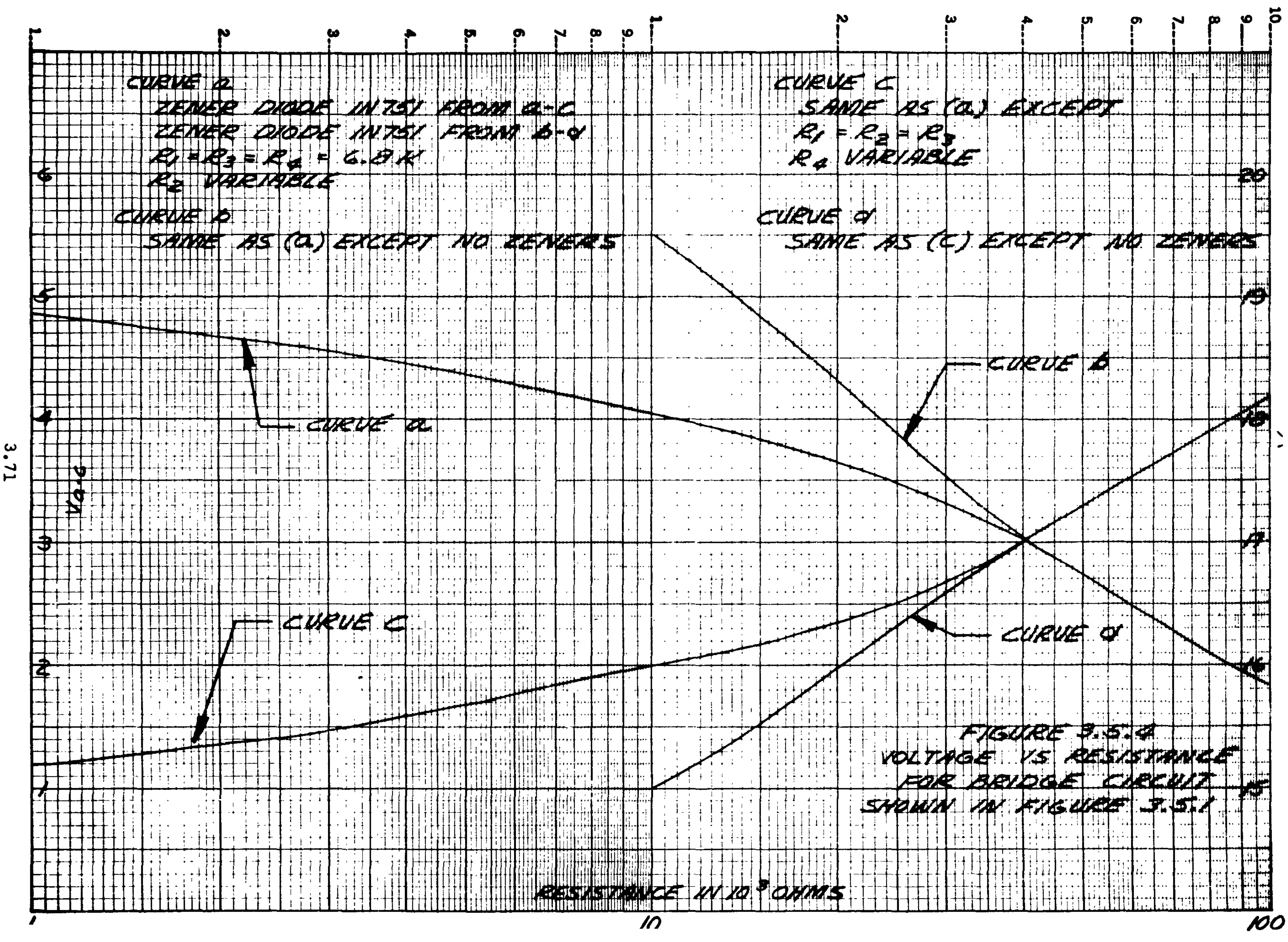


FIGURE 3.5.4
VOLTAGE VS RESISTANCE
FOR BRIDGE CIRCUIT
SHOWN IN FIGURE 3.5.1

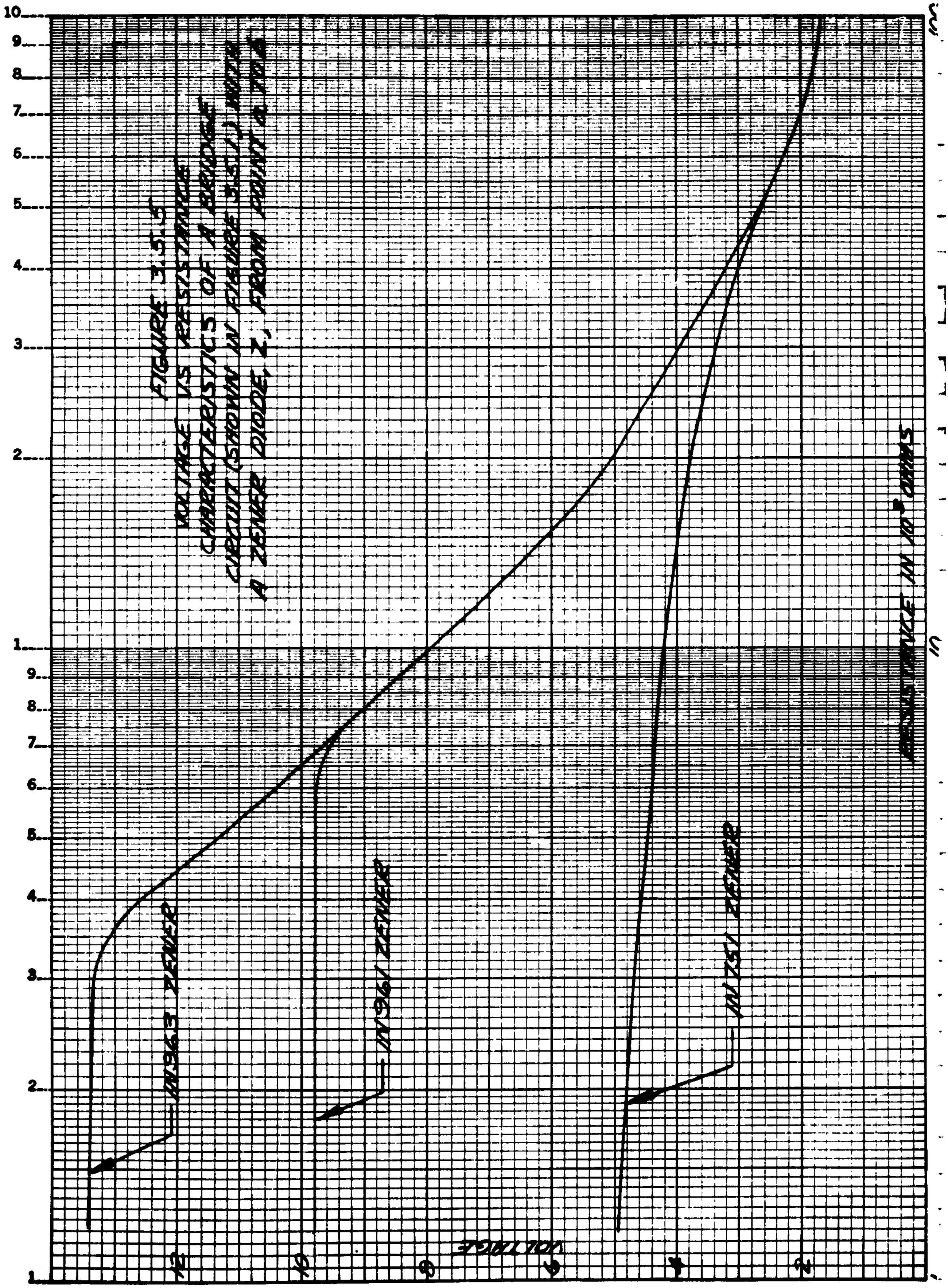


FIGURE 3.5.5
VOLTAGE VS RESISTANCE
CHARACTERISTICS OF A BRIDGE
CIRCUIT (SHOWN IN FIGURE 3.5.1)
A ZENER DIODE, Z, FROM POINT
1N963 ZENER
1N961 ZENER
1N751 ZENER
VOLTAGE
12
10
8
6
4
2
RESISTANCE IN OHMS
10
9
8
7
6
5
4
3
2
1
9
8
7
6
5
4
3
2
1

The effect of changing, R_2, on the voltage , V_{bc}, versus R_4 characteristics are as shown in Figure 3.5.6. This figure illustrates the fact that for null, $R_1R_3 = R_2R_4$. Because the tolerance on the resistors used was 10 percent, the measured value of R_1 and R_3 was about 6.2K. Thus for R_2 = 1 K, R_4 = 40K and R_4R_2 was equal to 4×10^7 R_1R_3 was about 3.97×10^7. For R_2 = 6.2 K, R_4 was equal to about 6.3 K at V_{bc} equal to zero volts and $R_2R_4 = 3.91 \times 10^7$. So within the limits of the measured resistance values, the equation $R_1R_3 = R_2R_4$ was satisfied at the points where V_{bc} was equal to zero volts.

Figure 3.5.7 shows the actual voltage across the diode versus the resistors R_4 as a function of R_2. This plot corresponds to the ones given in Figure 3.5.6, but indicates diode voltage instead of the bridge voltage, V_{bc}. The characteristic of the diode is quite obvious as the voltage across it goes positive. The diode has a very sharp break point at a positive voltage, about 0.5 volts.

Figure 3.5.2 shows the calculated V versus I curves for the diode used in the bridge for Figure 3.5.6 and 3.5.7.

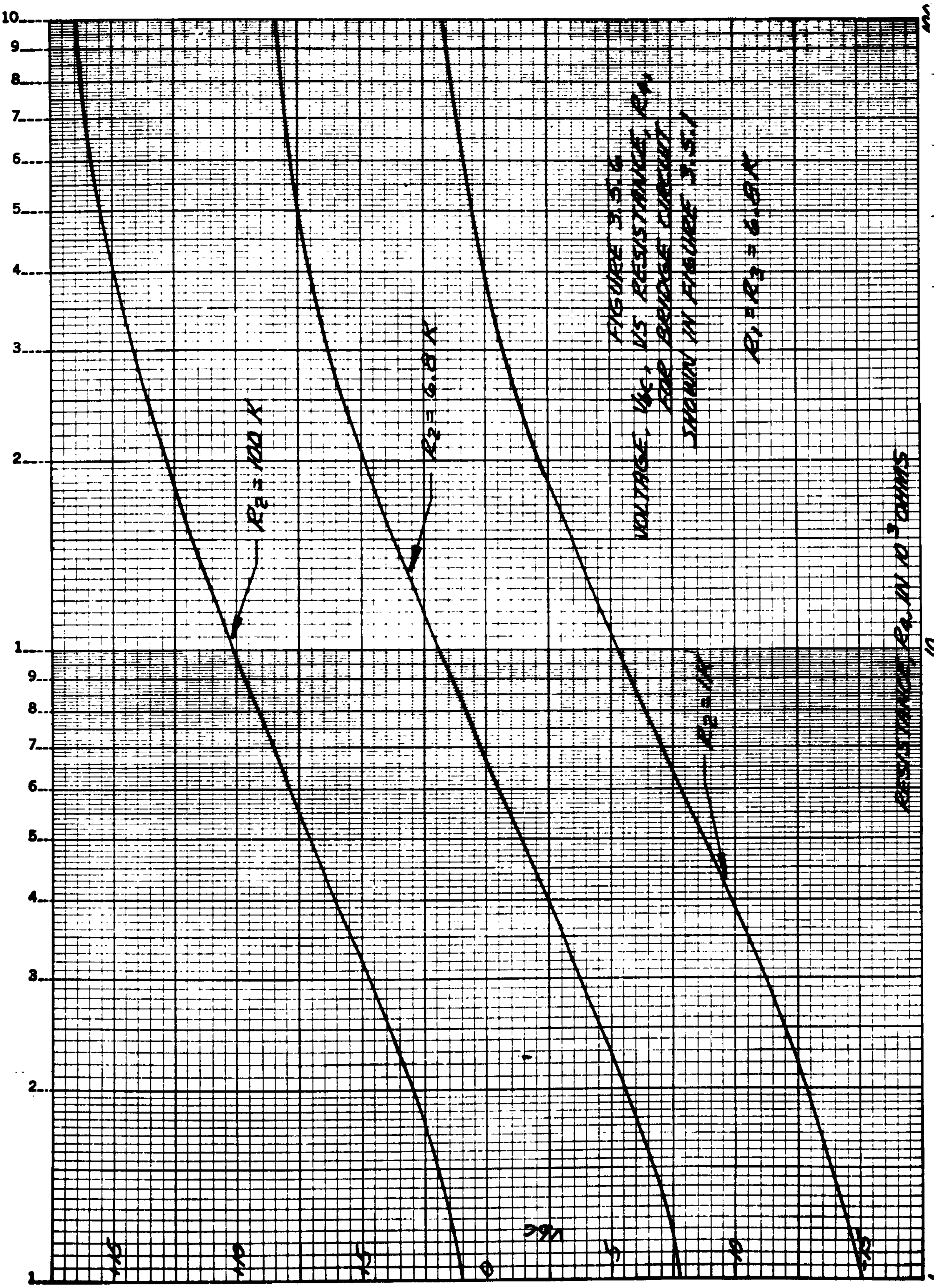


FIGURE 3.5.6
VOLTAGE, Vdc, VS RESISTANCE, R4
FOR BRIDGE CIRCUIT
SHOWN IN FIGURE 3.5.1
R1 = R3 = 6.8 K
R2 = 100 K
R2 = 6.8 K
R2 = 1 K
RESISTANCE, R4 IN 10^3 OHMS
Vdc
-15
-10
-5
0
5
10
15

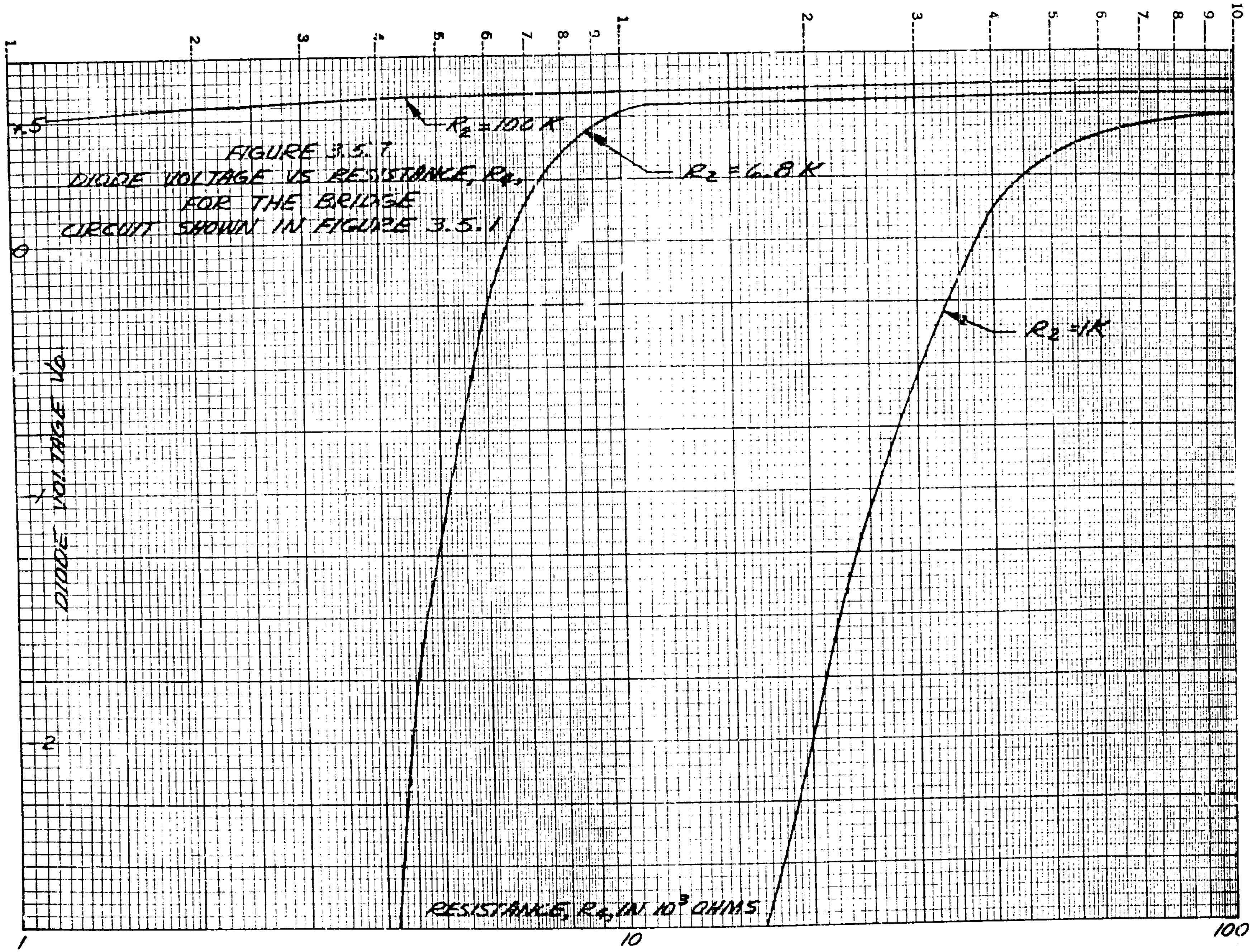


FIGURE 3.5.7
DIODE VOLTAGE VS RESISTANCE, R_4, FOR THE BRIDGE CIRCUIT SHOWN IN FIGURE 3.5.1

3.6 Oscillator Aging Tests

The aging tests on four compensated oscillators that was started during the first quarter is being continued. The aging data compiled to this time is very favorable. Very little aging has been observed in any of the oscillators. Some of the oscillators vary from one day to the next, but this is because the ambient temperature is not closely controlled when readings are taken. The change in ambient temperature will have an effect on the frequency of the oscillators because the compensation of all of the oscillators is not optimum at room temperature. Even though the readings taken from one time to the next may vary, if the curves are averaged over a period of time, it can be seen that the individual readings vary around a certain point or are varying at some rate with time. The aging data for the oscillators being tested is shown in Figure 3.6.1. Some of the original oscillators have been taken off of the aging tests. The data acquired from these oscillators was too erratic because the compensation was not adequate for the variations of room temperature. The changes of room temperature from day to day caused such large excursions in frequency that the aging effects were not apparent.

The method used to compensate each of the oscillators on the aging test is given in the table below.

Oscillator	Figure No.	Compensation Method
#1	3.6.2	Transistor
#3	3.6.3	Transistor
#5	3.6.4	Varicap
#6	3.6.5	Capacitor-Diode

Previous reports have the complete circuit diagrams for each of these compensated oscillators. The compensated oscillators that are being used for

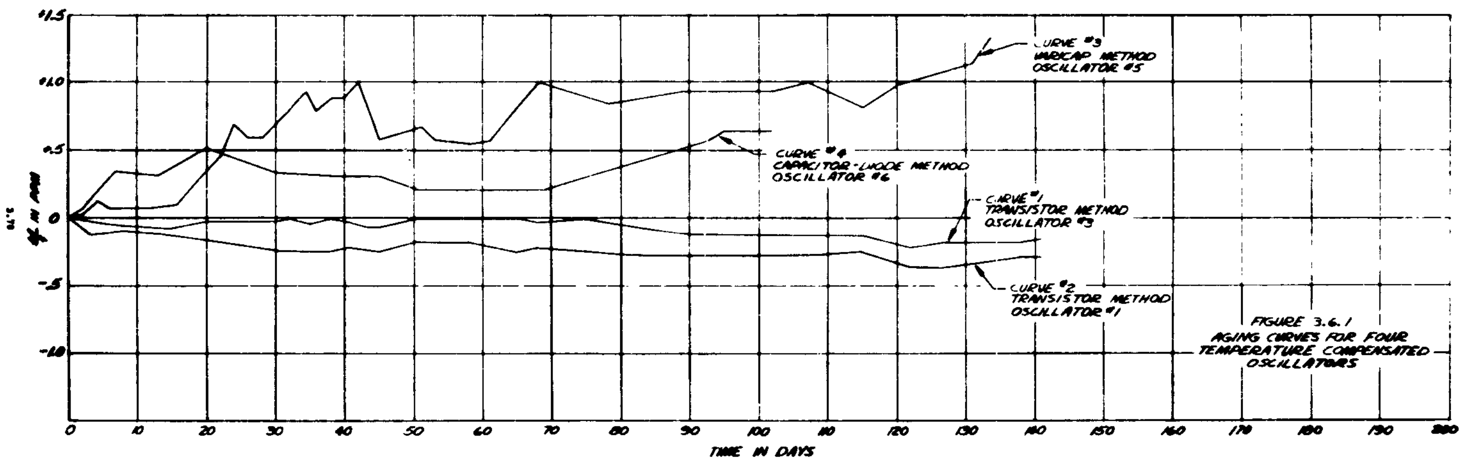


FIGURE 3.6.1
AGING CURVES FOR FOUR
TEMPERATURE COMPENSATED
OSCILLATORS

aging tests were not constructed from special components. The compensating networks were constructed using 10%, 1/10 watt carbon resistors and 10% thermistors. The biasing resistors for the oscillator transistor were also 1/10 10% carbon resistors. No special consideration was given to the temperature coefficient or stability characteristics of the components. Therefore some of the aging of the oscillators that has been observed may be due to changes in circuit component parameters other than the crystal. Future compensated oscillators that are intended for aging tests will be made from the best components available with special emphasis placed on component stability with time. This should produce aging characteristics for the oscillator that are similar to those of the crystal.

The aging oscillators were temperature cycled once during the second quarter of this contract. Figure 3.6.2, 3.6.3, 3.6.4 and 3.6.5 compare the original frequency-temperature curves to the curves taken during the aging tests. The frequency-temperature curves obtained during the second cycling agree very well with the original frequency-temperature curves that were obtained. The errors that are present between the two curves in each figure, except Figure 3.6.4, are very likely due to small temperature differentials. Also, if some the readings, either for the original curves, were taken before the temperature transient was completely gone, then apparent errors in the frequency at a given temperature will be observed. Until more temperature cycling tests are performed, it will be difficult to determine whether the errors in frequency that were observed were actual or due to error in temperature or to temperature transient.

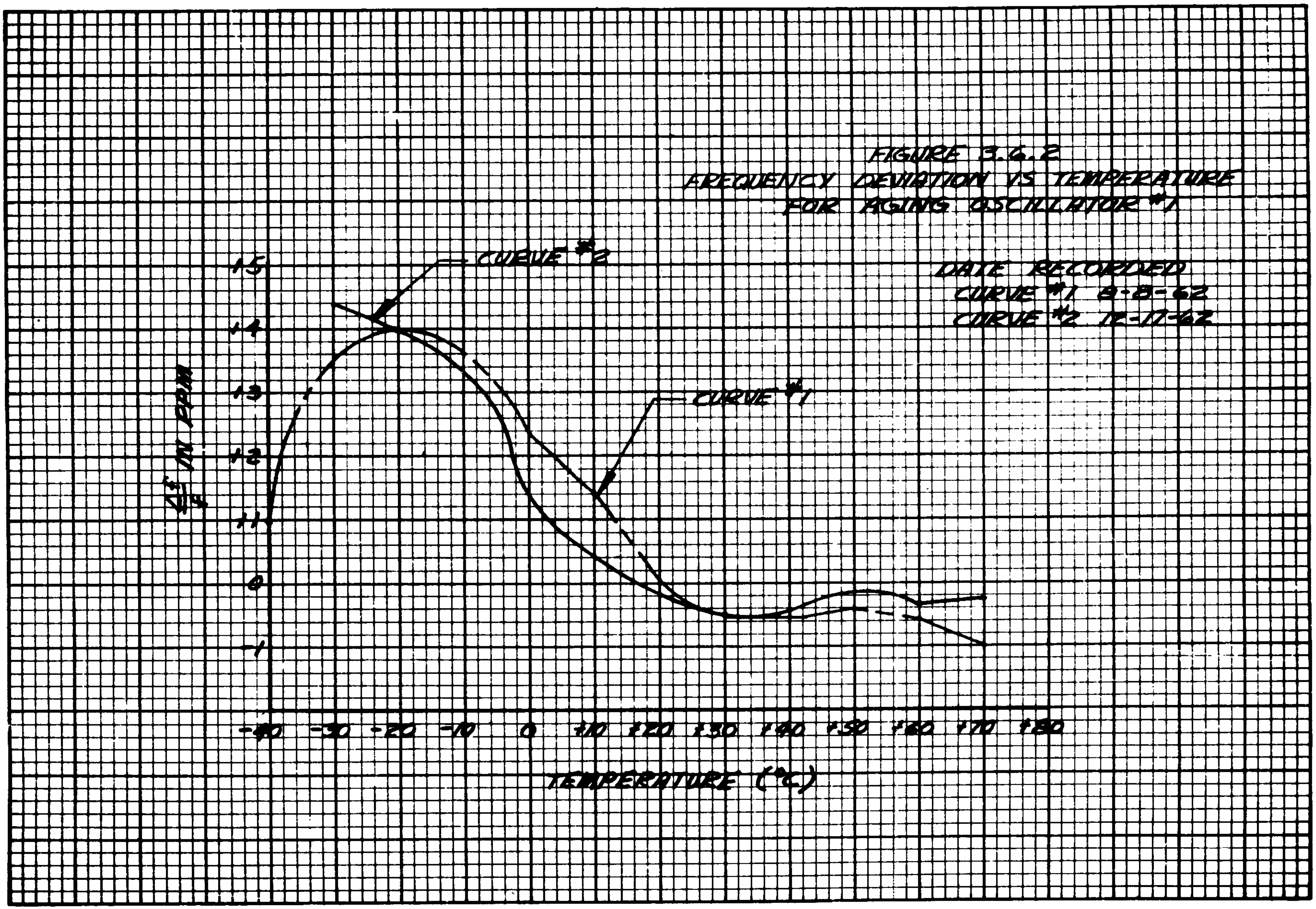


FIGURE 3.6.2
FREQUENCY DEVIATION VS TEMPERATURE
FOR AGING OSCILLATOR #1
DATE RECORDED
CURVE #1 8-8-62
CURVE #2 12-17-62
CURVE #2
CURVE #1
Δf/f IN PPM
+5
+4
+3
+2
+1
0
-1
-40
-30
-20
-10
0
+10
+20
+30
+40
+50
+60
+70
+80
TEMPERATURE (°C)

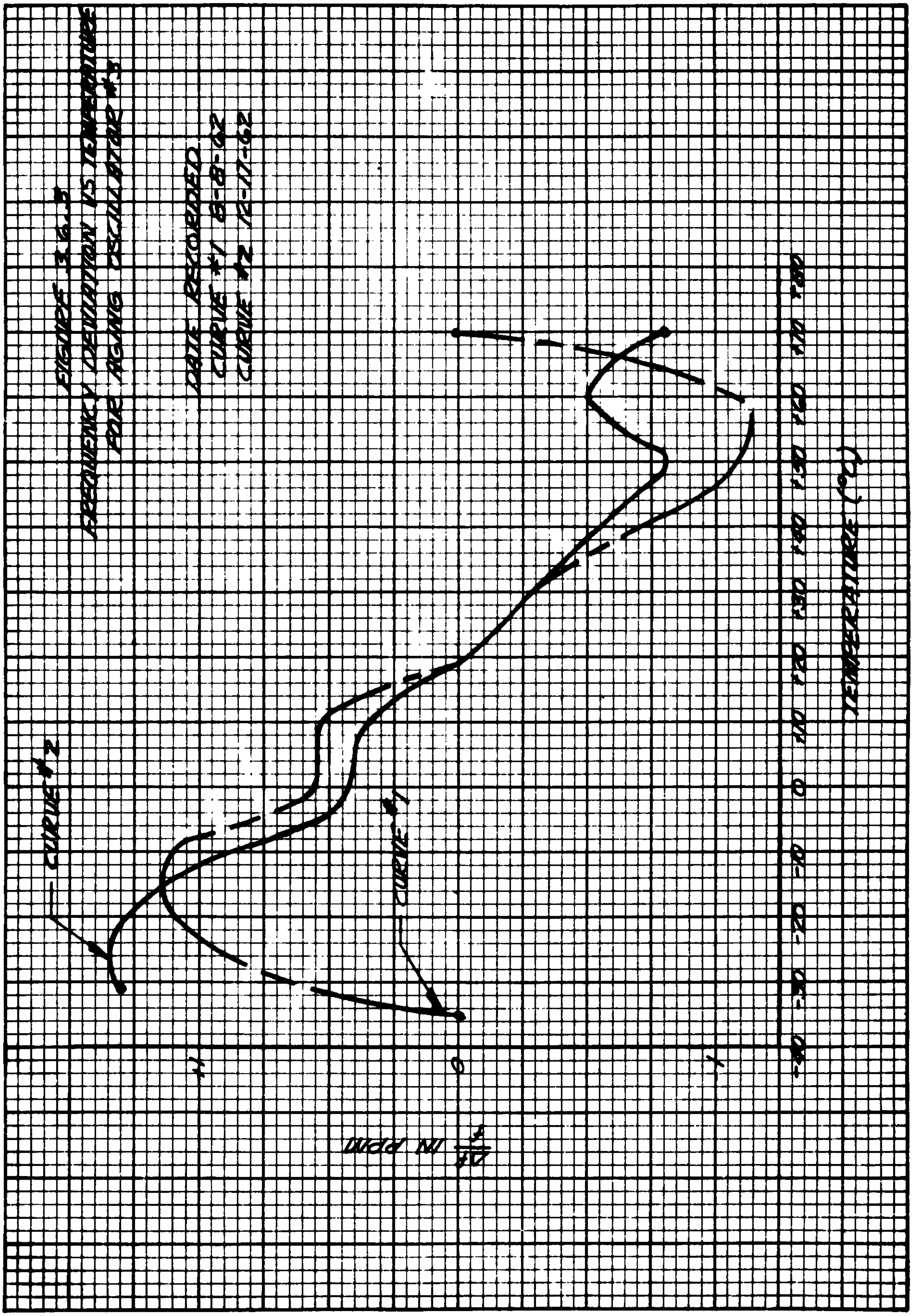


FIGURE 3.6.
FREQUENCY DEVIATION VS TEMPERATURE
FOR AGING OSCILLATOR #3
DATE RECORDED
CURVE #1 8-8-62
CURVE #2 12-17-62
CURVE #2
CURVE #1
+1
0
-1
$\frac{\Delta f}{f}$ IN PPM
-40 -30 -20 -10 0 10 20 30 40 50 60 70 80
TEMPERATURE (°C)

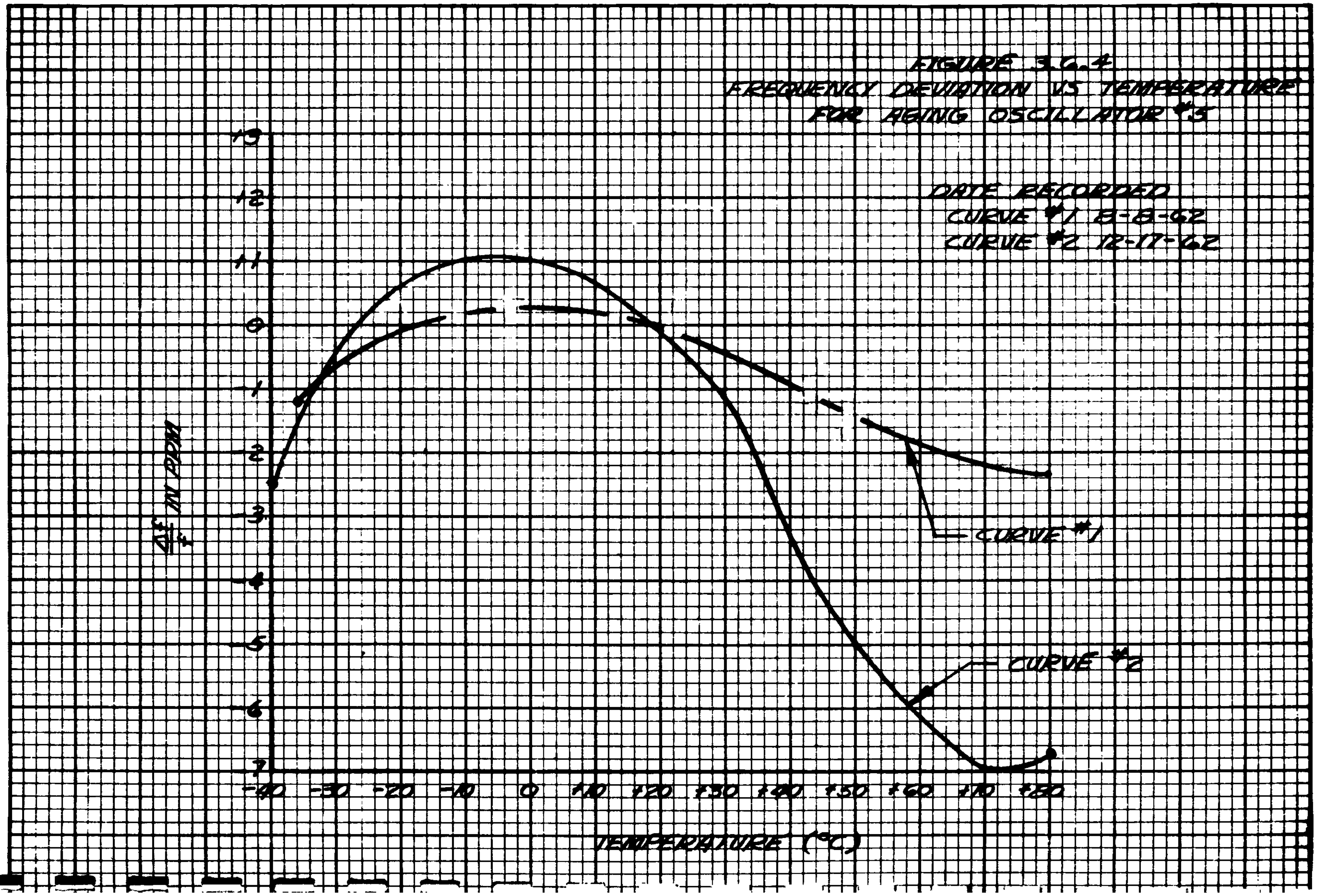


FIGURE 3.6.4
FREQUENCY DEVIATION VS TEMPERATURE
FOR AGING OSCILLATOR #5
DATE RECORDED
CURVE #1 8-8-62
CURVE #2 12-17-62
CURVE #1
CURVE #2
+3
+2
+1
0
-1
-2
-3
-4
-5
-6
-7
$\frac{\Delta f}{f}$ IN PPM
-40 -30 -20 -10 0 +10 +20 +30 +40 +50 +60 +70 +80
TEMPERATURE (°C)

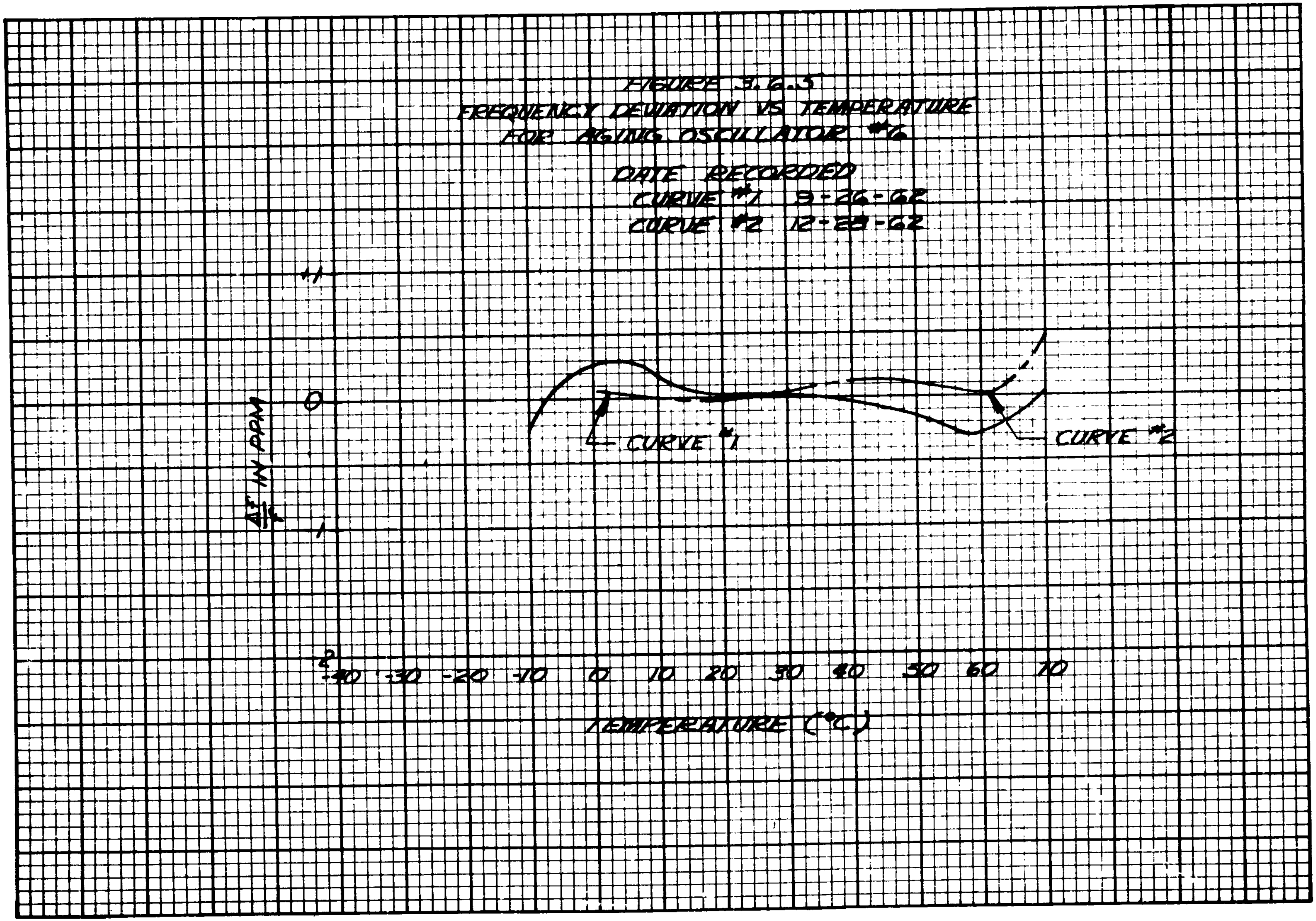


FIGURE 3.6.3
FREQUENCY DEVIATION VS TEMPERATURE
FOR AGING OSCILLATOR #6

The error between the two curves in Figure 3.6.4 cannot be explained in the above manner. It appears as if the thermistor controlling the high temperature end has either been shorted or open circuited. This is the only reasonable explanation for the difference between the two curves. At the completion of the aging curves, oscillator #5 will be dismantled and the cause for the error determined.

4.1 Conclusions

The compensation methods that appear to be the most promising for very accurate frequency-temperature compensation of crystal oscillators are the varicap and capacitor diode method. The binistor method has not been thoroughly evaluated because of the lack of appropriate binistor characteristics, therefore, for the present, the binistor method is not feasible. The transistor method requires more involved techniques than does the varicap and capacitor diode methods, although the aging characteristics of the transistor compensated oscillators appear to be the best. Aging data on a larger sample of compensated oscillators will have to be compiled before conclusive results are obtained.

The variety of techniques whereby control networks can be devised presents a selection of many different approaches to compensation of an oscillator using the same compensation method. Each control network seems to have certain advantages over other types for various conditions, such as the crystal angle of cut, temperature range, etc.

The method presented that eliminates the effect of B+ voltage variations on the frequency of the oscillator is very applicable. This technique, if proven to be completely satisfactory, will eliminate the need for accurately regulated voltages.

5.1 Personnel Associated with the Project

The following Engineering personnel have engaged in various activities in conjunction with the project during the report period.

PROJECT DIRECTOR

Dr. Darrell E. Newell, Ph.D. Approximate Hours - 18

Education: BSEE, Iowa State University, 1952
MSEE, State University of Iowa, 1956
Ph.D. in EE, State University of Iowa, 1958

Experience: From June 1961 to present - Dr. Newell is the Senior Engineer in charge of research, design and development of products within the Electronics Section. Representative projects include; development of new techniques in cryogenic liquid level measurement and flow measurement for missile and space applications, preliminary development of complete propellant management system for Saturn II vehicle, development of new techniques for temperature compensation of crystal oscillators, development of a new crystal type cryogenic thermometer and other internal sponsored development projects directed towards advance applications in space and missile technology.

From June 1959 to May 1961 - Associate Professor in the Research Section of the Electrical Engineering Department at the State University of Iowa. Some of the projects under his jurisdiction included:

1. Study of temperature compensation circuitry for quartz crystal oscillators.
2. Investigation of the short-term instability of regenerated dividers.
3. Investigation of mechanical refrigerator suitable for cooling quartz crystals.
4. Investigation of parametric amplification, oscillator, multiplication and conversion.
5. Nuclear Gyroscope Projects

From 1952 to 1959 - Dr. Newell was employed by Collins Radio Company, Cedar Rapids, Iowa. During this period when academic endeavors were pressing he was employed as a consultant and the remaining time as a Research Engineer in charge of such projects as propagation, excitation and function generator control problems.

1949 to 1952 - Transmission Engineer for WOI-AM-FM-TV

Professional Affiliations:

1. Member and Officer of Institute of Radio Engineers
2. Registered Professional Engineer of Iowa
3. Member of Iowa Academy of Science
4. Maintains First Class Radio - Television Commercial License

Patents:

1. Switching Circuitry
2. Automatic Frequency Control
3. Frequency Stabilizing Networks

Publications:

1. "Research Modulation" published by Collins Radio Co.
2. "An Investigation of Noise and Function Generators" published by Collins Radio Company.

PROJECT ENGINEER

Richard H. Bangert — Approximate Hours - 260

Education: AA, Keokuk Community College, 1958
BSEE, State University of Iowa, 1961
Graduate work towards MSEE, State University of Iowa

Experience: August 1961 to present - Mr. Bangert is the Project Engineer in charge of the Frequency Synthesis and Control Group. Projects under his direct supervision include:

1. Phase-Locked Frequency Dividers
2. Temperature Compensated Oscillators
3. Miniature Oscillators
4. Frequency Standards
5. 50 Megacycle Phase-Locked Loop System
6. Ultra-Stable Telemetering Oscillators
7. Research Study for Signal Corps Temperature Compensated Quartz Crystal Oscillators

February 1960 to August 1961 - Mr. Bangert worked as a graduate assistant in the Electrical Engineering Department at the State University of Iowa. Projects included; temperature compensation of quartz crystal oscillator, circuitry design for temperature compensation of quartz crystal oscillators, designed computer program for IBM 7070 to find a means of synthesizing temperature compensation networks.

Professional Affiliations: Member of Institute of Radio Engineers

Patents: 3 pending
Temperature Compensation of Quartz Crystal Oscillators

TECHNICIANS — Approximate Hours 463

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This contract is supervised by the Solid State and Frequency Control Division Electronics Components Department, USAERDL, Fort Monmouth, New Jersey. For further technical information, contact the Project Engineer, Mr. Stanley S. Schodowski, Telephone 535-2602 (New Jersey Area Code 201).

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THE BENDIX CORPORATION
PIONEER-CENTRAL DIVISION
Davenport, Iowa
FREQUENCY TEMPERATURE COMPENSATION TECHNIQUES
FOR QUARTZ CRYSTAL OSCILLATORS
by R. H. BANGERT

Report No. 2, Second Quarterly Report, 1 October to 31 December 1962. 93 pages including figures. Contract No. DA-36-039 SC-90782, Unclassified Report.

The approaches of circuit techniques for temperature compensation of oscillators which eliminate the need for precisely controlling the oscillator temperature environment is discussed.

Five different approaches are analyzed. The first method utilizes the change in capacitance of a back-biased diode with voltage, the second and third utilizes the change in capacitance of the collector-base junction of a transistor as the bias point changes, the fourth utilizes a "binistor" where the third junction is used as a back-biased diode, the fifth method uses the reactance changes exhibited by a forward-biased diode in parallel with a capacitor. Several new approaches to voltage control networks are discussed, including a bridge voltage and current control network that is applicable to both the varicap and capacitor-diode method.

Results of continued aging tests on the compensated crystal oscillators are also shown.

UNCLASSIFIED

1. Compensation
   Varicap
   Transistor
   Isolation Stage
   Binistor
   Capacitor-Diode
   Diode Voltage Control
   Switching
2. Crystal
3. Oscillators
4. Temperature
5. Stability
6. Aging

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